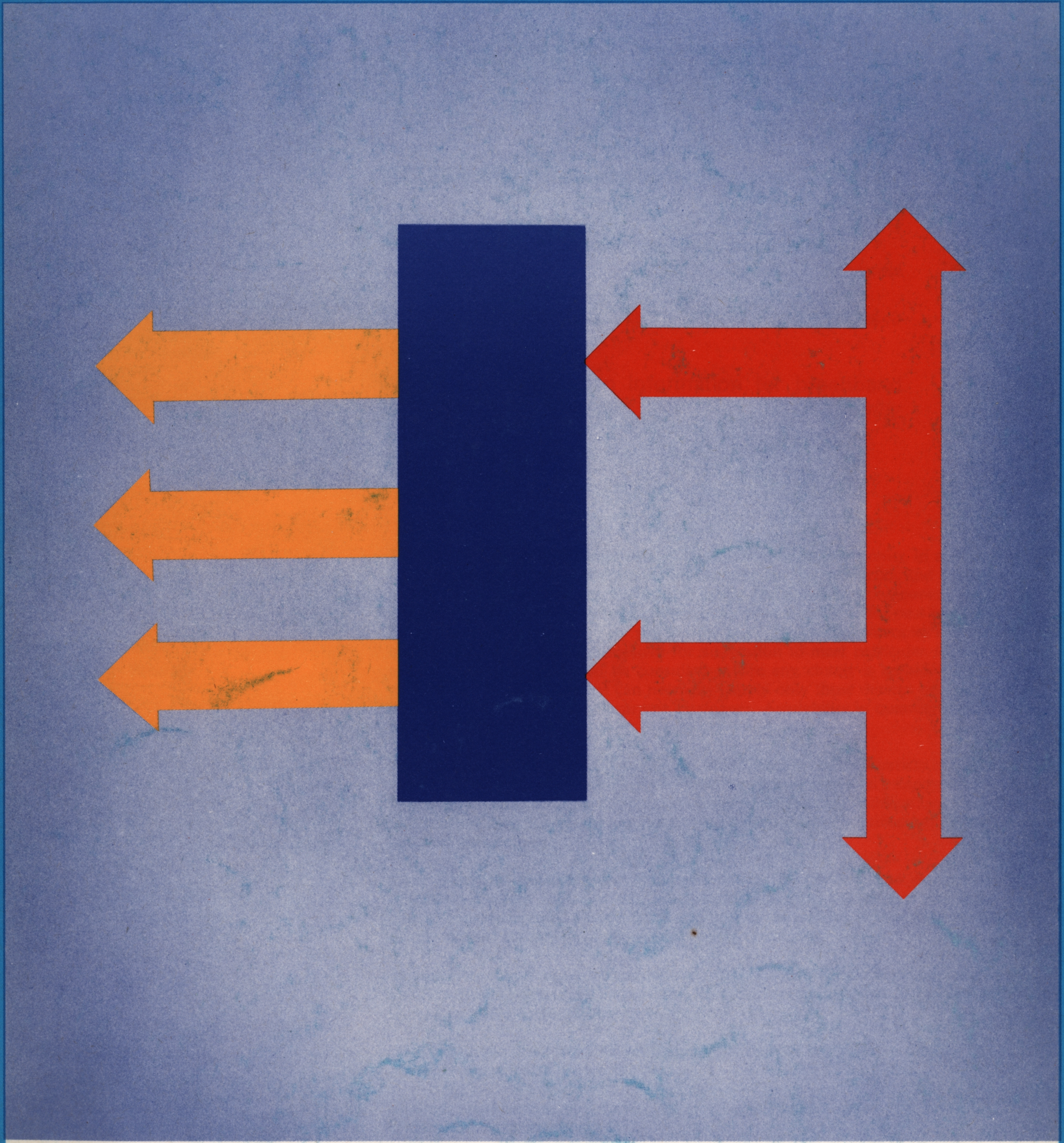
Mullard

Technical Communications

Volume 14 Number 138 April 1978



- IEC/IEEE data transmission bus interfaces
- Power strobing of bipolar read-only memories
- 20AX Hi-Bri colour tv picture tubes
- Design and application information for broadband solid-state noise sources

Mullard Technical Communications

ISSN 0027—3139

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Cover picture:

Representation of interface between digital systems. The need for the simple interconnection of devices in complex computer systems is becoming more and more important. This issue contains an article on the proposed IEC/IEEE standard data transmission interface.

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Editor:
Edmund G. Evans

Assistant Editor:
Michael J. Prescott

Design and Production:
Michael J. Rose

Technical Publications Department
Mullard Limited,
New Road, Mitcham,
Surrey, CR4 4XY

Made and Printed in England by
The Yale Press Ltd.,
Carmichael Road, London, S.E.25.

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IEC/IEEE data transmission bus interfaces

P.J. Jackson
Mullard Technical Publications Department

Various standards have been proposed for the unambiguous interconnection of electronic devices in digital systems. This article describes one such standard, which has been proposed by the IEC and is similar to an existing IEEE standard. The 16-line IEC/IEEE bus is described, together with the use of a new IC, the HEF4738V, which has been specifically designed for use in this bus interface system.

INTRODUCTION

The development of larger and more complex digital systems has led to a requirement for a simple method of interconnecting, or interfacing, electronic devices which may have widely varying operating speeds and data transmission rates. Various standards have been proposed for such interface systems, which would make it possible for any device to be connected to any other device by a simple 'plug-in' method. One such standard is defined in IEC publication 66 CO 22, and this standard is practically identical to IEEE standard 488-1975.

The proposed IEC standard bus interface is designed for use in digital systems in which the devices are not widely separated (in a laboratory for example).

This article describes in detail the IEC/IEEE standard bus (abbreviated to 'IEC bus' throughout), and explains its operation. Details are also given of the use of the HEF4738V, an IC newly developed by Philips specifically for use in this type of interface.

THE IEC BUS

The IEC bus consists of 16 identical lines, divided functionally into three groups. One group is used to carry data bytes and interface control messages, the second is used to control the transfer of data bytes between devices, and the third is used to 'manage' the interface system. Each of these groups is described in detail below.

Data bus

The data bus is a set of eight signal lines, designated DIO1 to DIO8 (data input/output 1 to 8), which carries the data bytes transferred between devices, and all interface control messages. All the information carried on these lines is in a bit-parallel byte-serial form, and is transferred asynchronously and bidirectionally.

Data byte transfer control bus

The data byte transfer control bus comprises three signal lines, designated DAV (data valid), NRFD (not ready for data), and NDAC (not data accepted). The DAV line is used to indicate the availability and validity of information on the DIO lines; the NRFD line is used to indicate the readiness of a device (or devices) to accept data; and the NDAC line is used to indicate the acceptance or non-acceptance of data by a device (or devices).

These three lines operate in a three-wire interlocked 'handshake' process, meaning that a specific sequence of signals must be exchanged on these lines during the transfer of a data byte.

Management bus

The management bus comprises five signal lines, completing the 16 lines of the IEC bus, and these five lines are used to control the entire interface system. The lines are designated ATN (attention), IFC (interface clear), SRQ (service request), REN (remote enable), and EOI (end or identify); these are described separately below.

Attention (ATN)

The ATN line is used to specify how data on the DIO lines is to be interpreted. If ATN is active, the information on the data bus is to be treated as a 7-bit interface command, to be decoded and operated on. If ATN is not active, the information on the data bus is to be treated as an 8-bit data byte.

Interface clear (IFC)

The IFC line is used to place the interface system, parts of which are contained in all interconnected devices on the IEC bus, in a known quiescent state.

Service request (SRQ)

The SRQ line is used by a device to indicate the need for service, and to request an interruption in the current sequence of events.

Remote enable (REN)

The REN line is used, in conjunction with other messages, to select between local (front or rear panel controls) and remote (messages from other devices) programming data for a device.

End or identify (EOI)

The EOI line is used by a device transmitting data to indicate the end of a multiple-byte transfer sequence; it can also be used by a controlling device, in conjunction with the ATN line, to execute a polling sequence (see later).

INTERFACING DEVICES WITH THE IEC BUS

Fig.1 shows in schematic form the connection of a device to the IEC bus. The various elements shown in this diagram are described below.

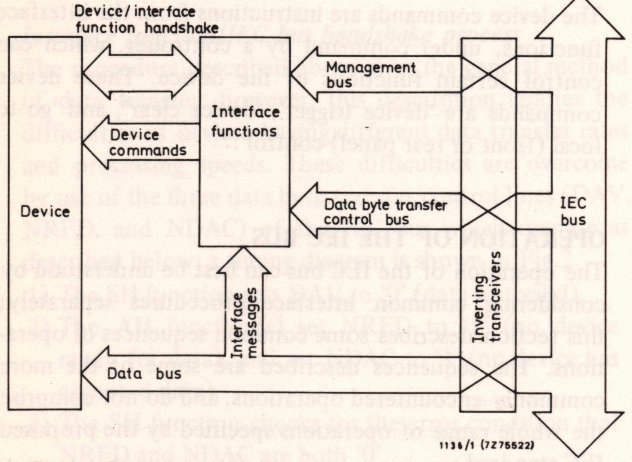


Fig.1 — Schematic diagram of the interface between a device and the IEC bus

Device

An effective communication link requires three basic elements: a device acting as a 'talker' (able to transmit information to another device); a device acting as a 'listener' (able to receive information from another device); and a device acting as a controller (able to address devices to listen or talk, and also able to send messages to control the interface). The four main categories of device are given in Table 1, with examples. Each device is interfaced with the IEC bus in the same way; it is connected to the data bus directly, and to the byte transfer control bus and the management bus via the interface functions (see later) as shown in Fig.1.

Interface functions

The interface functions are the elements of the system providing the operational facilities through which a device can receive, process, and send messages. The possible functions are listed in Table 2, and their modes of operation are defined by the proposed IEC standard. A brief description of each is given below.

TABLE 1
Categories of Device for a Data Communication System

Type of device	Example
Device able to talk only	Paper tape reader
Device able to listen only	Signal generator
Device able to talk and listen	Digital voltmeter
Device able to talk, listen, and control	Microcomputer

TABLE 2
Interface Functions Defined by the Proposed IEC Standard

Interface function	Symbol
Source handshake	SH
Acceptor handshake	AH
Talker function	T
Listener function	L
Service request function	SR
Remote/local function	RL
Parallel poll function	PP
Device clear function	DC
Device trigger function	DT
Controller function	C

Some of the material in this article originally appeared in 'Data transmission bus interfaces', New Electronics, Vol.11, No.2, January 24, 1978, pp.26 to 34.

Source handshake function (SH)

The SH function controls the initiation and termination of the transmission of a data byte on the DIO lines, using the DAV, NRFD, and NDAC lines to effect each transfer. The inclusion of this interface function means that the system designer has no need to include in a device a handshake procedure with the byte transfer control bus, as this is performed by the SH function.

Acceptor handshake function (AH)

The AH function guarantees the proper reception of a data byte by a device. An interlocked handshake sequence between an SH function and one or more AH functions (in separate devices) guarantees asynchronous data transfer, using the DAV, NRFD, and NDAC lines. The AH function may delay the initiation or termination of the transfer process until it is prepared to continue.

Talker function (T)

The T function enables a device acting as a talker to send data bytes (including status information) over the interface to other devices. This capability only exists when the device has been addressed to talk by a device acting as a controller. The extended talker (TE) function, using an extended address, is also defined by the standard.

Listener function (L)

The L function enables a device to receive data bytes (including status information) over the interface from other devices. This capability only exists when the device is addressed to listen by a controller. An extended listener (LE) function is also defined by the standard.

Service request function (SR)

The SR function makes it possible for a device to request service asynchronously from the controller of the interface. This function enables a device to interrupt the current sequence of events.

Remote/local function (RL)

The RL function indicates to the device that either input information from the front or rear panel controls (local), or from the interface (remote), are to be used.

Parallel poll function (PP)

The PP function makes it possible for the controller of the interface to receive requests for service from several devices simultaneously. Each device to be checked is assigned by the controller to a single DIO line, and when a parallel poll is initiated by the controller each of the specified devices sends a '1' or a '0' to indicate whether it requires service.

Device clear function (DC)

The DC function makes it possible for the controller to clear (initialise) a device, or a group of devices.

Device trigger function (DT)

The DT function enables the device to have its basic operation started either individually or as a member of a group of devices.

Controller function (C)

The C function enables a device to send device addresses, universal interface commands, and addressed commands to other devices over the interface. It also permits the conducting of parallel polls (see above) to determine which devices require service.

All the interface functions described above are fully specified by the proposed IEC standard, and their interconnection and interrelation are also specified, to simplify the task of the interface system designer.

Interface messages

When the ATN line of the IEC bus is active (see earlier), information on the data bus is treated by the interface functions as an interface message. This means that the information is decoded by the interface functions and acted on accordingly. An interface message may be an address which has been assigned to a device, to indicate that that device is to be used; an instruction to an addressed device; or a universal instruction to all devices.

Device/interface function handshake

The device/interface function handshake is the method of communication between the device and the interface function, specifically the SH and AH functions. As the handshake process between the interface functions and the IEC byte transfer control bus is performed by the interface functions, the device/interface function handshake can be very simple. It may consist of only two lines, or may be omitted completely in certain circumstances.

Device commands

The device commands are instructions from the interface functions, under command by a controller, which can control certain functions of the device. These device commands are 'device trigger', 'device clear', and 'go to local (front or rear panel) control'.

OPERATION OF THE IEC BUS

The operation of the IEC bus can best be understood by considering common interface procedures separately; this section describes some common sequences of operations. The sequences described are some of the more commonly encountered operations, and do not comprise the whole range of operations specified by the proposed IEC standard.

It should be noted that all the lines on the IEC bus are defined to be active low. In the following descriptions, therefore, a '1' represents the active state (low voltage level), and a '0' represents the inactive state (high voltage level).

Data byte transfer

During the transfer of a data byte over the interface from one device to another, the interface control device exercises overall control, and each transfer is performed using the handshake procedures between device and interface functions, and between interface functions and the IEC bus. The handshake between the device and the interface functions is specified by the system designer, while the handshake between the interface functions and the IEC bus is defined by the proposed IEC standard.

The proposed standard also specifies the coding of interface messages to be sent by the controller to the interface functions, but the coding of data bytes is left to the system designer.

General data byte transfer procedure

1) The controller sets ATN to '1'.
2) The controller sends the 'unlisten' command, which inhibits all current listener devices, over the DIO lines.
3) The controller sends over the DIO lines the address of the listener device which is to receive the data. More than one address can be sent consecutively if more than one device is to receive the same data.
4) The controller sends the address of the talker device which is to send the data to the listener or listeners; this device is enabled to send data as soon as ATN becomes '0'.
5) The controller sets ATN to '0'; serial data bytes are then transferred on the DIO lines from the currently enabled talker to all currently enabled listeners. Data can be sent until the controller again sets ATN to '1'. If the talker is sending a specific number of bytes, it may optionally set EOI to '1' while sending the last byte.

Interface function/IEC bus handshake process

The procedure described above gives the general method of data transfer; however, this description ignores the difficulties of devices having different data transfer rates and processing speeds. These difficulties are overcome by use of the three data byte transfer control lines (DAV, NRFD, and NDAC) of the IEC bus which operate as described below; a timing diagram is shown in Fig.2.

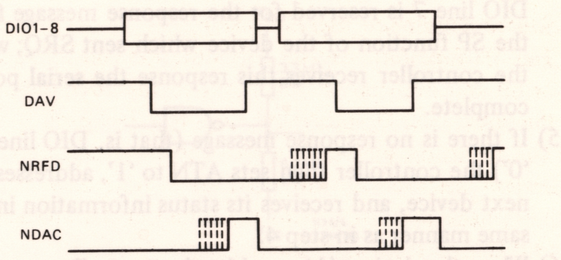


Fig.2 — Timing diagram of the data byte transfer handshake procedure

1) The SH function sets DAV to '0' (data not valid).
2) The AH function(s) set NRFD to '1' (no device ready for data), and set NDAC to '1' (no device has accepted data).
3) The SH function checks for the error condition that NRFD and NDAC are both '0'.
4) The talker device then sets a data byte on the DIO lines, and delays to ensure that the data is settled.
5) When the listener devices have indicated readiness to accept the first data byte, NRFD goes to '0'.
6) On sensing that NRFD is '0', the SH function of the talker device sets DAV to '1', to indicate that the data on the DIO lines is settled and valid.
7) The AH function of the first listener device sets NRFD to '1' to indicate that it is no longer ready, and then the listener accepts the data. Any other addressed listeners follow, at their own rates.
8) The AH function of the first listener device sets its NDAC output to '0' to indicate that it has accepted the data; NDAC remains at '1' as long as any AH function is driving it at this level.
9) When the AH functions of all the addressed listener devices have set their NDAC outputs to '0', the NDAC line goes to '0'.
10) The SH function of the talker device, having sensed that NDAC is '0', sets DAV to '0'. This indicates that data on the DIO lines is no longer to be considered valid.
11) The talker device can now place the next data byte on the DIO lines, and the process is repeated from step 4 to step 10. It should be noted that after step 10 the DAV, NRFD, and NDAC lines are in the same states as they are after step 2.

Serial poll

A serial poll procedure is performed by a controller, usually whenever a device sets the SRQ line of the IEC bus to a '1'. In a serial poll the interface controller checks each device in turn until it finds the one that sent the SRQ message; this device then sends status information to the controller, which can then service it. The operational sequence is given below.

1) The controller sets ATN to '1'.
2) The controller sends the 'unlisten' message to prevent other devices from listening to status information sent to the controller.
3) The controller sends the 'serial poll enable' message. This puts the interface into serial poll mode, during which addressed devices send status information rather than data.
4) The controller sends the talk address of the first device, and sets ATN to '0'; the device then sends status information on DIO lines 1 to 6 and DIO line 8.

DIO line 7 is reserved for the response message from the SP function of the device which sent SRQ; when the controller receives this response the serial poll is complete.

5) If there is no response message (that is, DIO line 7 is '0') the controller then sets ATN to '1', addresses the next device, and receives its status information in the same manner as in step 4.
6) When the device addressed by the controller sets DIO line 7 to '1', the controller sets ATN to '1' and sends the 'serial poll disable' message, ending the poll.

The device which sent the SRQ message then removes this request and can be serviced by the controller.

Parallel poll

Periodically, the interface controller may conduct a parallel poll of devices. In this process, the controller assigns (configures) each device to a particular DIO line, and instructs each device whether to use a '1' or a '0' as a service request on that line. The sequence of events is given below.

1) The controller sets ATN to '1' and EOI to '0'.
2) The controller sends the listen address of a device which is to be assigned to a DIO line.
3) The controller sends the 'parallel poll configure' message, which enables the addressed device to be configured.
4) The controller sends the 'parallel poll enable' message; bit 4 of this message specifies the sense of the response or the assigned DIO line, and bits 1 to 3 specify, in binary code, the DIO line on which the response is to be sent.
5) The controller sends the 'unlisten' message, ending the configuration routine.
6) The controller repeats steps 2 to 5 until all devices have been configured as required.
7) The controller sets EOI to '1'. Each configured device then places its service request message on its assigned DIO line.

As there are eight DIO lines, eight devices can be accessed during a parallel poll. This number can be increased indefinitely by assigning more than one device to each line, so that the line value represents an AND or an OR combination of requests depending on the sense ('1' or '0') of the response specified by the controller.

The configuration of a device can be removed by the controller by sending the 'parallel poll unconfigure' message

Placing devices in forced remote control

1) The controller sets ATN and REN to '1'.
2) The controller sends the 'local lock-out' message, which disables the 'return-to-local' buttons of all devices.
3) The controller sends the listen addresses of all devices required to be in the remote control state. Each address sent disables the local controls of each addressed device. If REN goes to '0', all devices addressed in this way will return to local control.

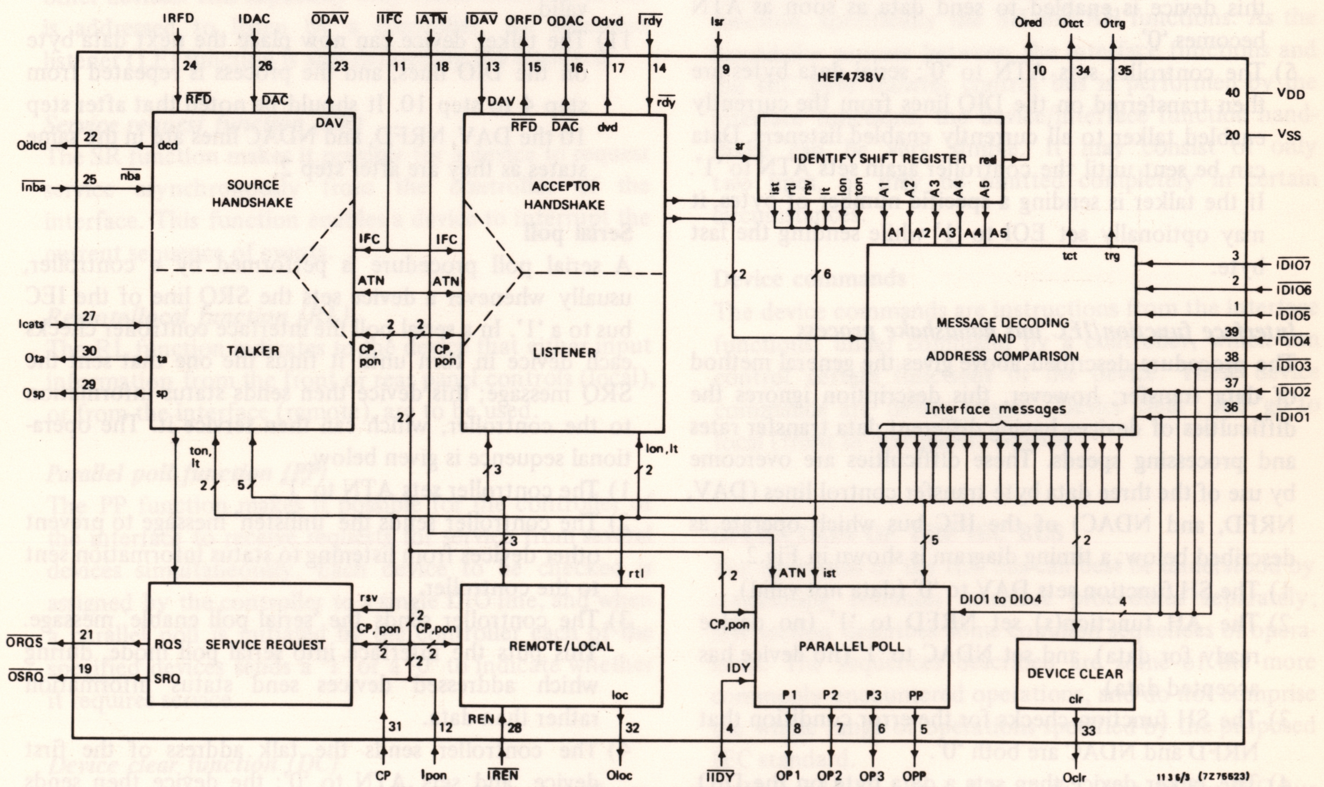
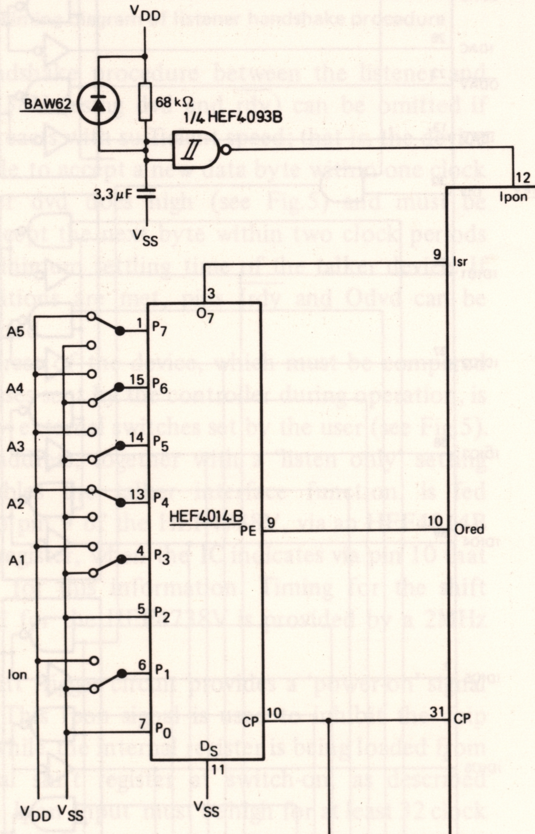

HEF4738V
SOURCE HANDSHAKE
ACCEPTOR HANDSHAKE
IDENTIFY SHIFT REGISTER
TALKER
LISTENER
MESSAGE DECODING AND ADDRESS COMPARISON
Interface messages
SERVICE REQUEST
REMOTE/LOCAL
PARALLEL POLL
DEVICE CLEAR
IRFD
IDAC
ODAV
IIFC
IATN
IDAV
ORFD
ODAC
Odvd
Irdy
Isr
Ored
Otct
Otrg
VDD
VSS
Odcd
Inba
Icats
Ota
Osp
ORQS
OSRQ
IDIO1
IDIO2
IDIO3
IDIO4
IDIO5
IDIO6
IDIO7
IDY
CP
Ipon
IREN
Oloc
OP1
OP2
OP3
OPP
Oclr
1136/3 (7Z75623)

Fig.3 — Block diagram of the HEF4738V interface IC

THE HEF4738V INTERFACE IC AND THE IEC BUS

The HEF4738V LOCMOS IC has been developed by Philips specifically for use in IEC bus interface systems. It includes all the interface functions described in earlier sections except the controller function (C), the extended talker function (TE), and the extended listener function (LE). A block diagram of the IC is shown in Fig.3; it should be noted that in this figure and later ones an output from the HEF4738V is preceded by an 'O', and an input to the IC is preceded by an 'I'. The HEF4738V is intended to be used as the 'interface functions' block of Fig.1, for interfacing talker devices, listener devices, and devices able to both talk and listen.

In the following application examples, all the IEC bus-driver lines must be terminated with resistors to V_{SS} and V_{DD}; a typical example is shown in Fig.4. It should be noted that some bus drivers include termination resistors. All unused inputs of the HEF4738V must be connected to V_{SS}.


VDD
BAW62
68 kΩ
1/4 HEF4093B
3,3 µF
VSS
Address identification
A5
A4
A3
A2
A1
Ion
HEF4014B
VDD VSS
2 MHz Oscillator

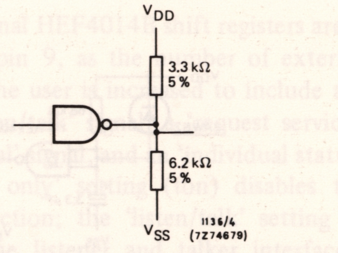

VDD
3,3 kΩ 5%
6,2 kΩ 5%
VSS
1136/4 (7Z74679)

Fig.4 — Typical line termination circuit

Using the HEF4738V with a listener device

Fig.5 shows the connection of the HEF4738V to a device in a basic listener configuration; the serial and parallel poll functions are not implemented. The DIO lines of the IEC bus are connected both to the device (for data) and to the message decoding block of the HEF4738V (for interface messages). The other lines on the IEC bus necessary for this configuration (DAV, NRFD, NDAC, ATN, and IFC) are connected to the

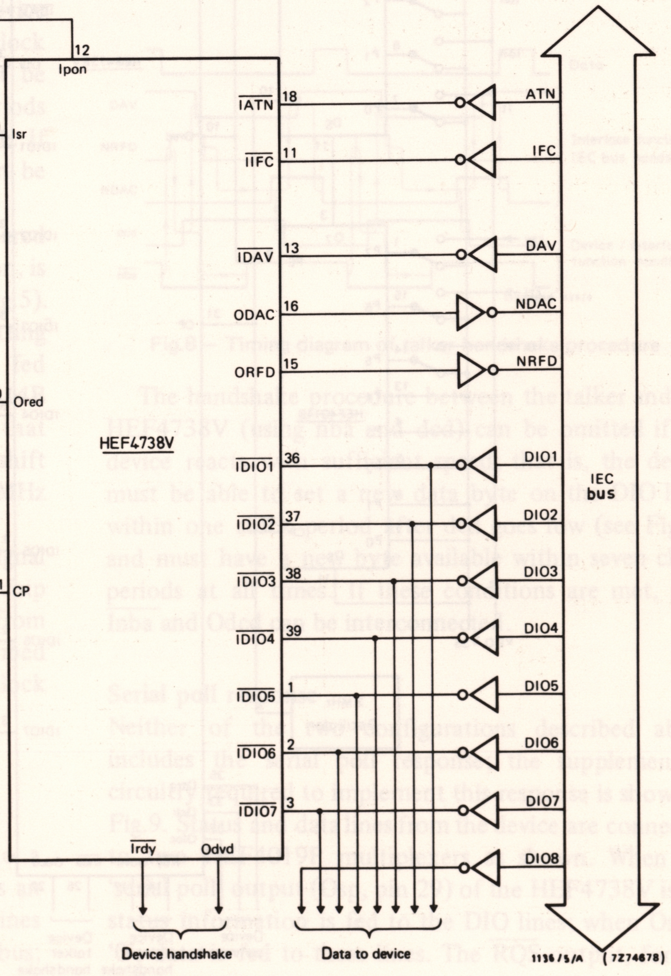

Ipon
Isr
Ored
CP
HEF4738V
IATN
IIFC
IDAV
ODAC
ORFD
IDIO1
IDIO2
IDIO3
IDIO4
IDIO5
IDIO6
IDIO7
Irdy
Odvd
ATN
IFC
DAV
NDAC
NRFD
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
IEC bus
Device handshake
Data to device
1136/5/A (7Z74678)

Fig.5 — Basic listener configuration

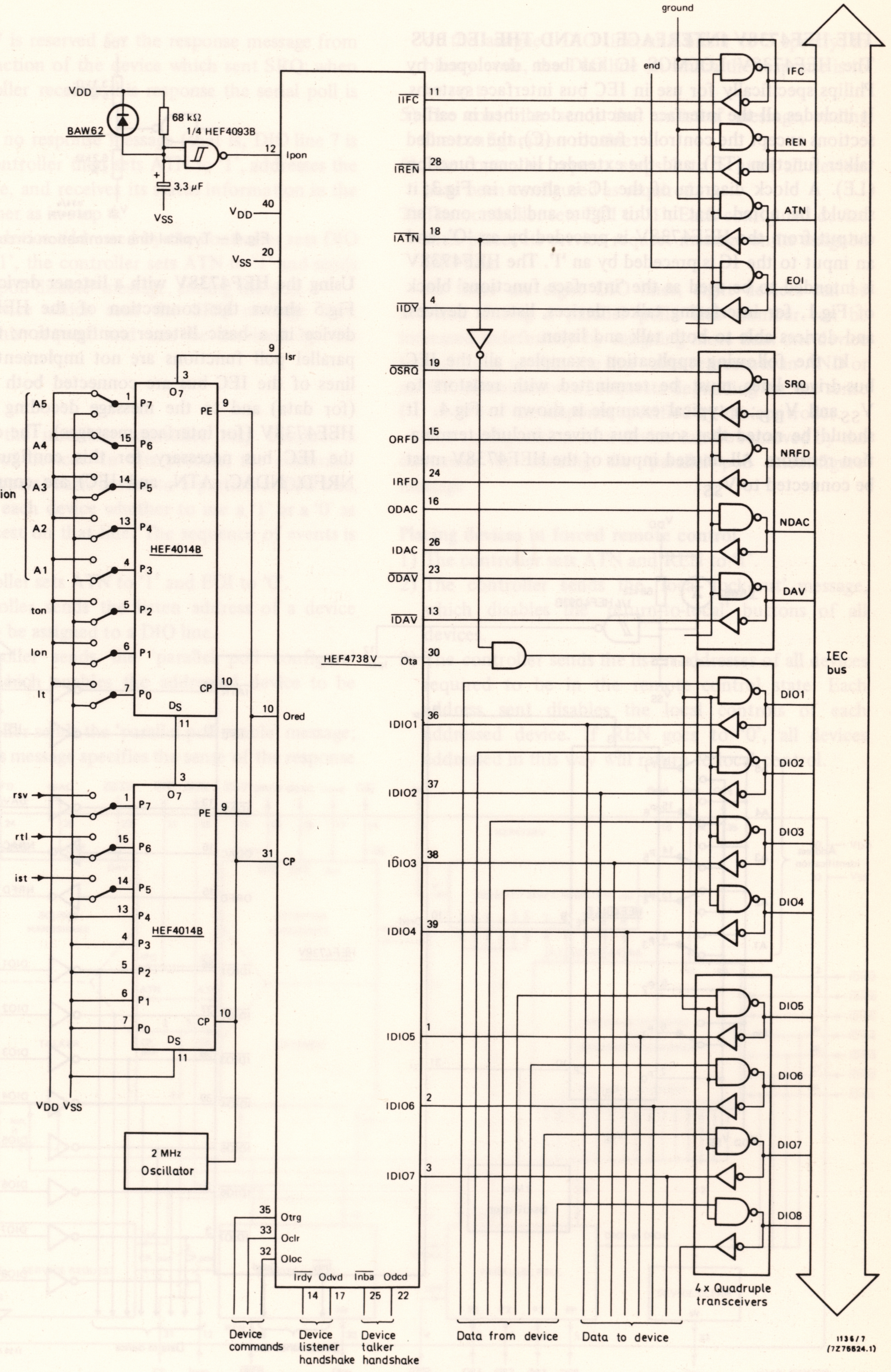

ground
end
IFC
REN
ATN
EOI
SRQ
NRFD
NDAC
DAV
IEC bus
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
VDD
BAW62
68 kΩ
1/4 HEF4093B
3,3 μF
VSS
Ipon
Isr
Ored
CP
HEF4738V
Address identification
A5
A4
A3
A2
A1
ton
lon
lt
HEF4014B
rsv
rtl
ist
2 MHz Oscillator
Otrg
Oclr
Oloc
Irdy Odvd Inba Odcd
Device commands
Device listener handshake
Device talker handshake
Data from device
Data to device
4 x Quadruple transceivers
1135/7 (7Z76824.1)

Fig.7 – Combined talker and listener configuration

appropriate pins of the IC as shown. The only connections between the IC and the device are two lines for the device/interface function handshake and three lines for device commands; these five lines are dvd (data valid device), $\overline{\mathrm{rdy}}$ (ready for new data), clr (device clear), $\overline{\mathrm{loc}}$ (go to local), and trg (device trigger). The dvd and rdy handshake lines are synchronised with the DAV, NRFD, and NDAC handshake lines, as shown in Fig.6. The handshake between the HEF4738V and the IEC bus is performed automatically by the IC.

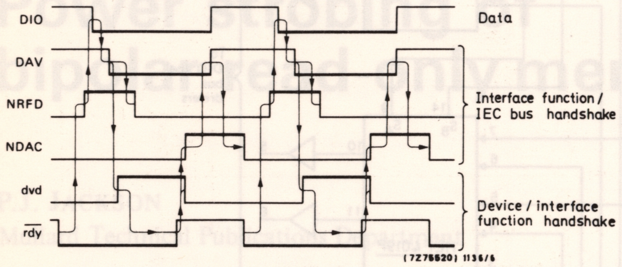

DIO
DAV
NRFD
NDAC
dvd
rdy
Data
Interface function / IEC bus handshake
Device / Interface function handshake
(7Z76820) 1135/6

Fig.6 – Timing diagram of listener handshake procedure

The handshake procedure between the listener and the HEF4738V (using dvd and rdy) can be omitted if the device reacts with sufficient speed; that is, the device must be able to accept a new data byte within one clock period after dvd does high (see Fig.5) and must be ready to accept the next byte within two clock periods plus the minimum settling time of the talker device. If these conditions are met, pins I$\overline{\mathrm{rdy}}$ and Odvd can be interconnected.

The address of the device, which must be compared with addresses sent by the controller during operation, is specified by external switches set by the user (see Fig.5). The 5-bit address, together with a 'listen only' setting which disables the talker interface function, is fed serially into pin 9 of the HEF4738V, via an HEF4014B 8-bit shift register, when the IC indicates via pin 10 that it is ready for this information. Timing for the shift register and for the HEF4738V is provided by a 2MHz oscillator.

A Schmitt trigger circuit provides a 'power-on' signal to the IC. This Ipon signal is used to inhibit the chip functions while the internal register is being loaded from the external shift register at switch-on, as described above. The Ipon input must be high for at least 32 clock pulses after switch-on.

Using the HEF4738V with a device acting as a talker and listener

Fig.7 shows the connection of the HEF4738V to a device able to talk and listen. This configuration is an extension of the basic listener. Two sets of data lines connect the device with the DIO lines of the IEC bus; one set to get data into the device, and one set to get data out.

Two external HEF4014B shift registers are connected in series to pin 9, as the number of external settings available to the user is increased to include a 'talk only' signal, a 'listen/talk' signal, a 'request service' signal, a 'return to local' signal, and an 'individual status' signal.

The 'talk only' setting (ton) disables the listener interface function; the 'listen/talk' setting (lt) selects subsets of the listener and talker interface functions (defined by the proposed IEC standard); the 'request service' setting (rsv) enables the interface to perform service request functions when it is high; the 'return to local' setting (rtl) enables remote/local control switching; and the 'individual status' setting (ist) inhibits the parallel poll response, if the ist value is not equal to the sense of the parallel poll response fixed by the 'parallel poll enable' message from the controller.

The device command lines and the listener handshake lines between the HEF4738V and the device are the same as those shown in Fig.5, and two additional lines have been added to perform the talker handshake. These two lines are $\overline{\mathrm{nba}}$ (new byte available) and dcd (don't change data), and as before are synchronised with DAV, NRFD, and NDAC (see Fig.8) by the IC.

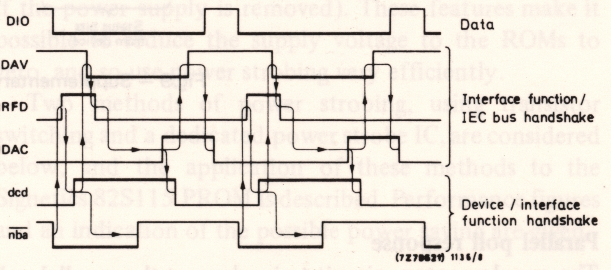

DIO
DAV
NRFD
NDAC
dcd
nba
Data
Interface function / IEC bus handshake
Device / interface function handshake
(7Z76822) 1135/8

Fig.8 – Timing diagram of talker handshake procedure

The handshake procedure between the talker and the HEF4738V (using $\overline{\mathrm{nba}}$ and dcd) can be omitted if the device reacts with sufficient speed; that is, the device must be able to set a new data byte on the DIO lines within one clock period after dcd goes low (see Fig.8), and must have a new byte available within seven clock periods at all times. If these conditions are met, pins I$\overline{\mathrm{nba}}$ and Odcd can be interconnected.

Serial poll response

Neither of the two configurations described above includes the serial poll response; the supplementary circuitry required to implement this response is shown in Fig.9. Status and data lines from the device are connected to two HEF4019P multiplexers as shown. When the 'serial poll' output (Osp, pin 29) of the HEF4738V is '1', status information is fed to the DIO lines; when Osp is '0', data is fed to these lines. The $\overline{\mathrm{RQS}}$ output, for the poll response, is connected via the multiplexer to DIO line 7 as described earlier. .

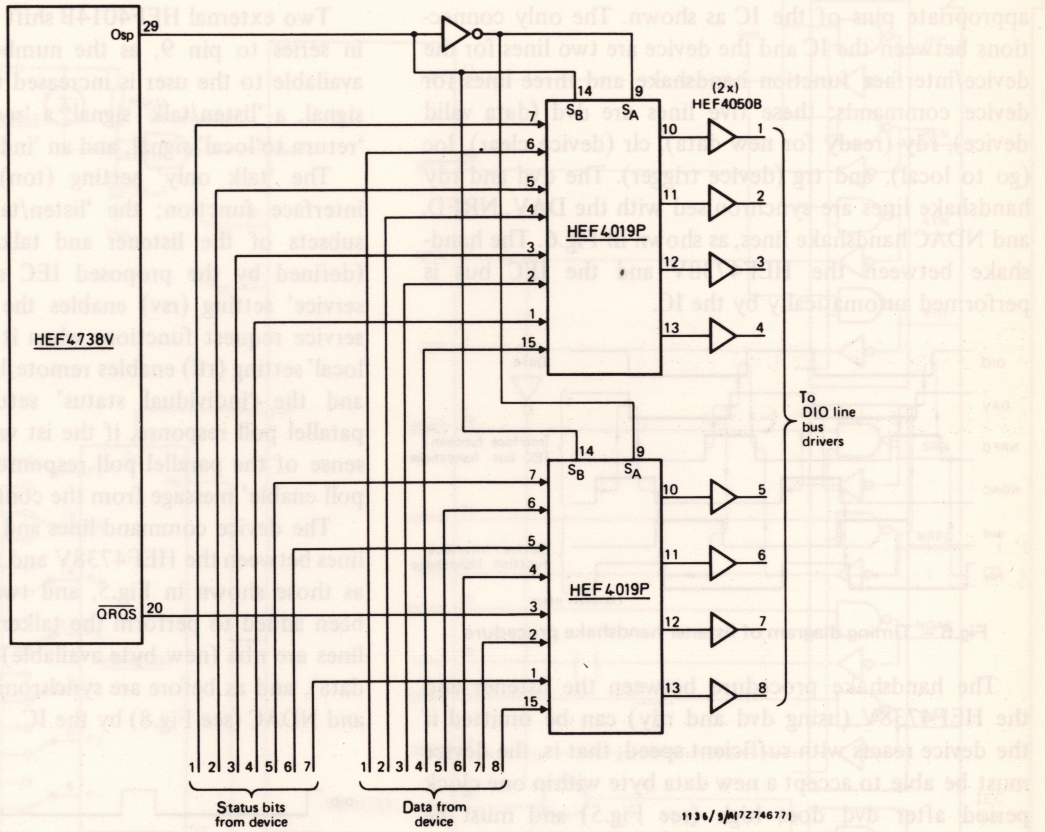


Fig.9 – Supplementary circuit for serial poll response

Parallel poll response

The supplementary circuit to implement the parallel poll response is shown in Fig.10. The Signetics 74154 IC is a BCD-to-decimal decoder. When the PP output of the HEF4738V goes to '1', the P_1, P_2, and P_3 outputs select one of the DIO lines for the poll response. As described earlier, the binary coding of P_1, P_2, and P_3 is fixed by the controller, which sends the 'parallel poll enable' message containing the coding information. This information is stored by the PP function of the HEF4738V until a parallel poll is initiated.

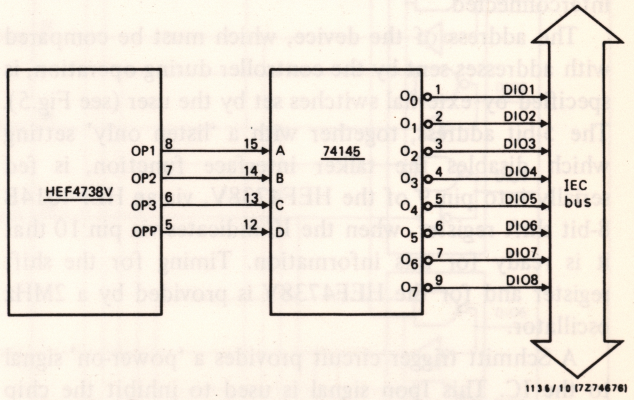


Fig.10 – Supplementary circuit for parallel poll response.

Power strobing of bipolar read-only memories

P.J. JACKSON
Mullard Technical Publications Department

The development of large memory systems, using modern high-density ICs, has emphasised the importance of reducing power consumption in the system for economic reasons. One method of reducing consumption is power strobing, which entails the removal of the positive supply voltage to an IC while it is not being accessed. This article describes two power strobing methods, and their application to the Signetics 82S115 bipolar PROM. Performance figures and possible power savings are given.

INTRODUCTION

Modern memory technology is leading to the development of larger and faster IC memory systems, and this in turn has led to a need for power economy in order to use the systems economically. One method of reducing the power consumption of a memory system, while retaining a reasonable operating speed, is power strobing. In this method, the average power consumption is reduced by applying the positive supply voltage to the memory ICs only while they are being accessed, and removing it while they are unused.

Bipolar read-only memories (ROMs) are particularly suitable for the application of power strobing, because they have low access times, relatively high power consumption compared with other memories, and are non-volatile (that is, they retain their stored information if the power supply is removed). These features make it possible to reduce the supply voltage to the ROMs to zero, and so use power strobing very efficiently.

Two methods of power strobing, using transistor switching and a dedicated power strobe IC, are considered below, and the application of these methods to the Signetics 82S115 PROM is described. Performance figures and an indication of the possible power saving are given.

D.C. PARAMETERS

Before implementing a power strobing system, it is necessary to consider the behaviour of the d.c. input and output parameters of the memory IC to be used, particularly when the supply voltage is reduced to zero.

The input impedance must remain high, and must not change significantly over the extended supply voltage range (0 to 5V). The output leakage currents must also remain within limits, both with and without a supply voltage, to ensure that the outputs are truly off when they are not enabled. It is therefore convenient to define several parameters to be checked, and these are given in Table 1.

A.C. PARAMETERS

A general power strobing circuit for one memory IC is shown in schematic form in Fig.1, and this circuit is used to define the a.c. parameters given in Table 2 and shown in Fig.2.

This article is based heavily on technical information supplied by L.W. McClish, Signetics Corporation, Sunnyvale, California, USA.

TABLE 1
D.C. Parameters for ROMs to be used with Power Strobing

Parameter	Definition
I_{ILM}	Input current, low level applied, maximum supply voltage*
I_{IH0}	Input current, high level applied, supply voltage removed
I_{IHM}	Input current, high level applied, maximum supply voltage*
I_{OLH0} †	Output leakage current, high level applied, supply voltage removed
I_{OLHM} †	Output leakage current, high level applied, maximum supply voltage*
I_{OLLM}	Output leakage current, low level applied, maximum supply voltage*

†For open-collector devices

*Normally given in published data

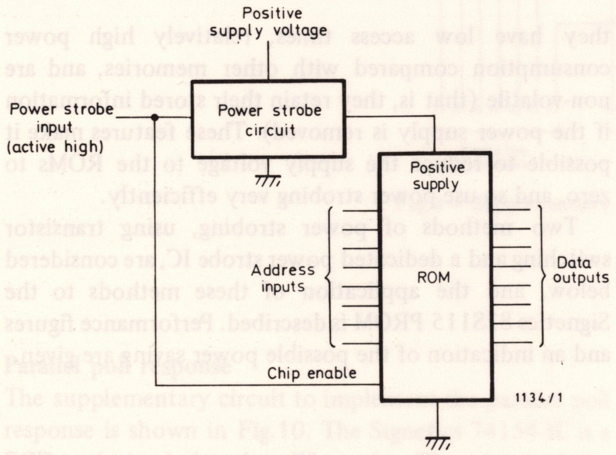


Fig.1 – Schematic diagram of general power strobing circuit

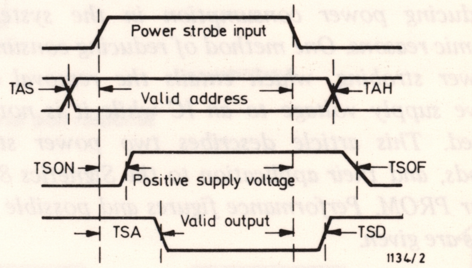


Fig.2 – Timing waveforms for the circuit of Fig.1

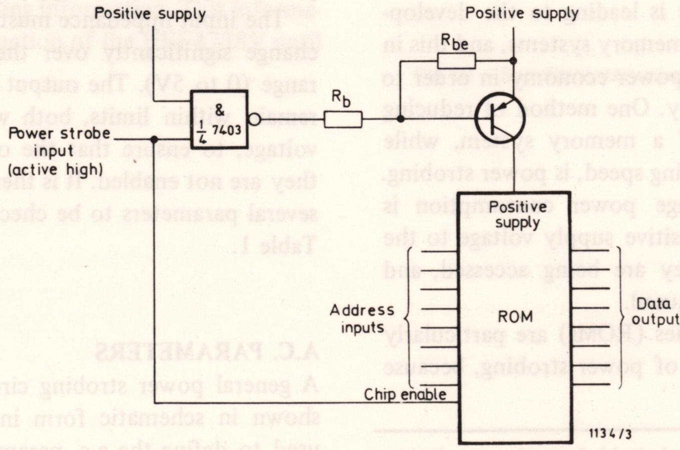


Fig.3 – Power strobing circuit using a saturated pnp switch

TABLE 2
A.C. Parameters for Power Strobing Circuits

Parameter	Description
TSA (Strobe access time)	Time interval between the active edge of the power strobe input and a valid data output.
TSD (Strobe disable time)	Time interval between the negative edge of the power strobe input and the disabling of the output.
TAS (Address-to-strobe set-up time)	Time interval between the active edge of a valid address signal and the active edge of the power strobe input.
TAH (Address-to-strobe hold time)	Time interval between the negative edge of the power strobe input and the active edge of the next valid address signal.
TSO_N (Strobe to power on)	Time interval between the active edge of the power strobe input and the positive edge of the supply voltage.
TSO_F (Strobe to power off)	Time interval between the negative edge of the power strobe input and the negative edge of the supply voltage.

All times measured between 50% points of waveform edges (see Fig.2)

METHODS OF POWER STROBING

The 'power strobe circuit' section of Fig.1 can have various forms, and two of these are described below.

Saturated pnp switching

A power strobing circuit using a saturated pnp switch is shown in Fig.3. The power strobe input is tied to the (active HIGH) chip-select pin of the ROM to give faster memory turn-off when the supply is removed. If the ROM chip-select pin is active LOW, the NAND gate (¼ 7403) should be replaced by an AND gate (¼ 7409); the power strobe input then becomes active LOW.

Transistor TR_1 should be chosen for high switching speed, low saturation voltage, high current gain (large h_{fe}), and a maximum collector current rating well above the supply current rating of the ROM. The value of resistor R_{be} is not critical, but should be about 5kΩ. The value of R_b can be calculated from:

$$R_b = \frac{10 \times (\text{supply voltage} - V_{be\,sat} - 0.4)}{\text{ROM supply current consumption}}\ \Omega,$$

where $V_{be\,sat}$ is the base-emitter saturation voltage of TR_1. The positive supply voltage should be the sum of 5V (the nominal ROM supply voltage) and the collector-emitter saturation voltage ($V_{CE\,sat}$) of TR_1.

This saturated switch configuration provides control of the ROM supply voltage without requiring an additional supply voltage.

Use of a dedicated power strobing IC

A power strobing circuit using a dedicated quadruple power strobe IC, for example the Harris HD-6600, is shown in Fig.4. In this circuit, the strobe IC selectively applies the supply voltage to four ROM ICs. The power strobe input signal is active LOW, and the active-LOW chip-enable pins of the ROMs are tied to this, as in the previous circuit, to speed up memory turn-off when the supply is removed. It should be noted that a separate +12V supply is required for this circuit.

APPLICATION OF POWER STROBING TO THE SIGNETICS 82S115 PROM

The Signetics 82S115 is a 4096-bit field-programmable bipolar ROM organised as 512 bytes, each of 8 bits. It is fully TTL-compatible, and includes tri-state outputs and two complementary chip-enable pins; these pins can be used for memory expansion and power strobing. Further details of the 82S115 can be found in the published data. It should be noted that the 'strobe' pin of the IC controls an output register, and has no connection with power strobing.

As described in an earlier section, the input and output leakage currents of the PROM must be checked before power strobing is implemented, to ensure that they remain LOW when the supply voltage is removed. Measurements made on a curve tracer with the supply removed show that both I_{H0} and I_{OLH0} (see Table 1) have values less than those obtained with the supply voltage connected.

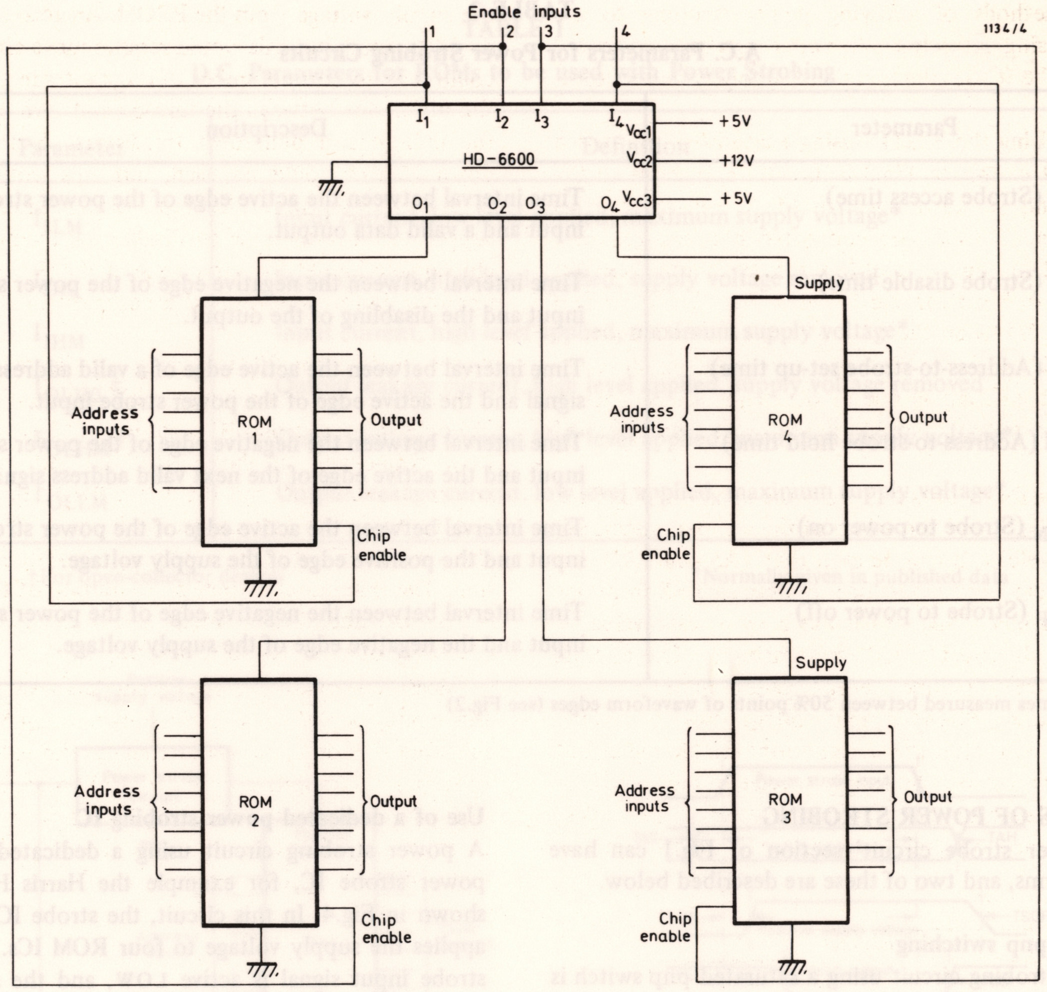


Fig.4 – Power strobing circuit using a dedicated IC

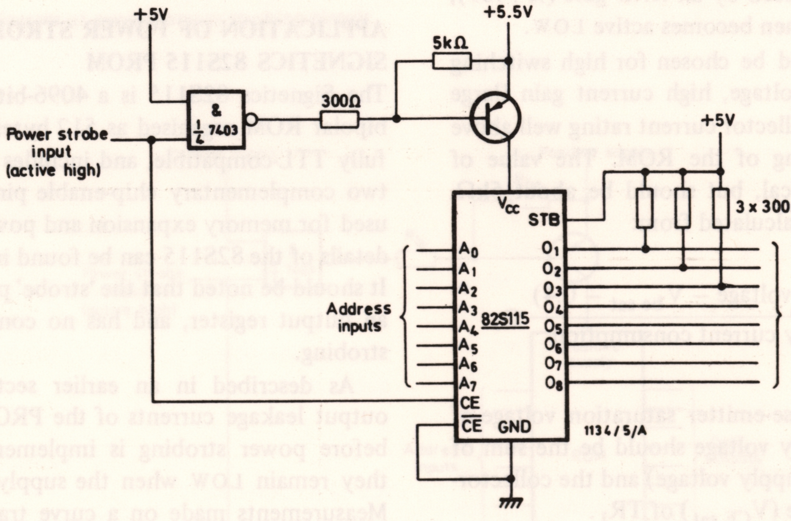


Fig.5 – Power strobing the 82S115 using a saturated pnp switch

Two methods of applying power strobing to the 82S115, using saturated pnp switching and a dedicated power strobe IC, are described in the following sections.

Power strobing the 82S115 using a saturated pnp switch

The circuit shown in Fig.3 is directly applicable to the 82S115, and is shown again in Fig.5. Pull-up resistors with values of 300Ω are connected between the +5V supply and the output pins (only three of these resistors are shown in Fig.5 for clarity) to ensure that these pins go to logic '1' when the IC is turned off. If a number of 82S115 ICs are wire-ORed together these resistors can be omitted, as long as one of the memories is enabled, because the outputs would always be at a well-defined logic level.

The waveforms obtained from the circuit of Fig.5 are shown in Fig.6, and the values of the a.c. parameters are listed in Table 3. It can be seen that TAS and TAH (see Table 2) were both set to 0ns. Increasing TAS from 0ns does not affect TSA, which has a worst-case value of 100ns for all possible address transitions. The address generation was performed using a 'gallop' pattern.

The positive PROM supply voltage rises to its 50% level about 35ns after the power strobe enable signal, but it takes over 1μs for the supply voltage to fall to 50% of its peak value after the power strobe signal goes LOW. This is because no pull-down circuit is used to remove the supply voltage from the PROM. An active pull-down could be used, but this would require more circuitry and could lead to current spikes during switching because of the difference between the turn-on and turn-off times of the pull-up and pull-down transistors. A passive pull-down resistor could be used, but this would increase power consumption. The best way of increasing the supply turn-off speed is to disable the memory via the chip-enable line at the same time as the power supply is removed; in this way turn-off is complete in 30ns.

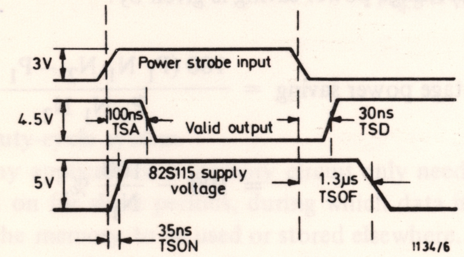


Fig.6 – Timing waveforms for the circuit of Fig.5

Power strobing the 82S115 using a dedicated IC

A method of power strobing the 82S115 using the Harris HD-6600 power strobe IC is shown in Fig.7. The active-LOW chip-enable of the 82S115 is used, tied to the power strobe input, and the active-HIGH chip-enable is tied to +5V. The internal strobe input of the PROM is also tied to +5V, to ensure a transparent mode of operation. The maximum current consumption of the 82S115 is 185mA, and this is safely below the 200mA drive capability of each HD-6600 output.

Measurements of the a.c. parameters were taken from this circuit, and the results are shown in Fig.8, and listed in Table 4. For these measurements, the recommended operating conditions of the HD-6600 were maintained, and pull-up resistors (each of 300Ω) were connected between the PROM outputs and the +5V supply; only three of these pull-up resistors are shown in Fig.7, for clarity.

POWER SAVINGS IN POWER STROBE SYSTEMS

The power savings in memory systems using power strobing depend on both the memory organisation, and on the duty cycle of the memory ICs, that is the ratio of the time the IC is on in a system cycle to the total system cycle time. These factors are considered next.

TABLE 3

A.C. Parameter Values for the Circuit of Fig.5

Parameter	Maximum value
TSA (Strobe access time)	100ns
TSD (Strobe disable time)	30ns
TAS (Address-to-strobe set-up time)	0ns
TAH (Address-to-strobe hold time)	0ns
TSON (Strobe to power on)	35ns
TSOF (Strobe to power off)	1.2μs

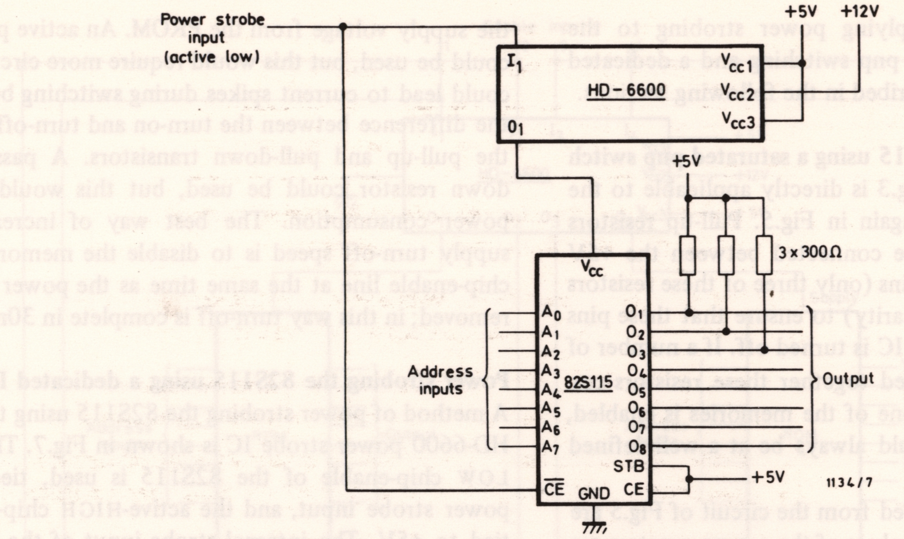

Power strobe input (active low)
+5V
+12V
I1
HD-6600
Vcc1
Vcc2
Vcc3
O1
+5V
3 x 300Ω
Vcc
A0
A1
A2
A3
A4
A5
A6
A7
Address inputs
82S115
O1
O2
O3
O4
O5
O6
O7
O8
Output
STB
+5V
CE
GND
CE
1134/7

Fig.7 – Power strobing the 82S115 using a power strobe IC

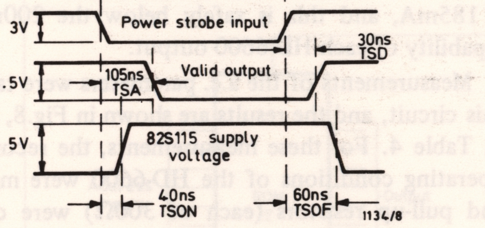

3V
Power strobe input
30ns
TSD
4.5V
105ns
TSA
Valid output
5V
82S115 supply voltage
40ns
TSON
60ns
TSOF
1134/8

Fig.8 – Timing waveforms for the circuit of Fig.7

Word-organised memory system

Consider the memory system shown in Fig.9. This consists of N_1 rows of ROMs, each row containing N_2 ROMS; as each ROM is organised as W bytes of B bits each, the complete system contains N_1W bytes each of N_2B bits.

Individual bytes are accessed by power strobing a row of ROMs on, and then selecting an address. If only one of the N_1 rows of ROMs is on at a time, the power saving compared with a system without power strobing is given by:

$$\text{Power saving} = P_1 N_1 N_2 - P_1 N_2,$$

$$= P_1 N_2 (N_1 - 1),$$

where P_1 is the power consumption of one memory IC. The percentage power saving is given by:

$$\text{Percentage power saving} = \frac{100\,(P_1 N_1 N_2 - P_1 N_2)}{P_1 N_1 N_2},$$

$$= 100 - \frac{100}{N_1}\,\%.$$

The power saving therefore increases as the number of rows of ROMs in the memory system increases.

TABLE 4

A.C. Parameter Values for the Circuit of Fig.7

Parameter	Maximum value
TSA (Strobe access time)	105ns
TSD (Strobe disable time)	30ns
TAS (Address-to-strobe set-up time)	0ns
TAH (Address-to-strobe hold time)	0ns
TSON (Strobe to power on)	40ns
TSOF (Strobe to power off)	60ns

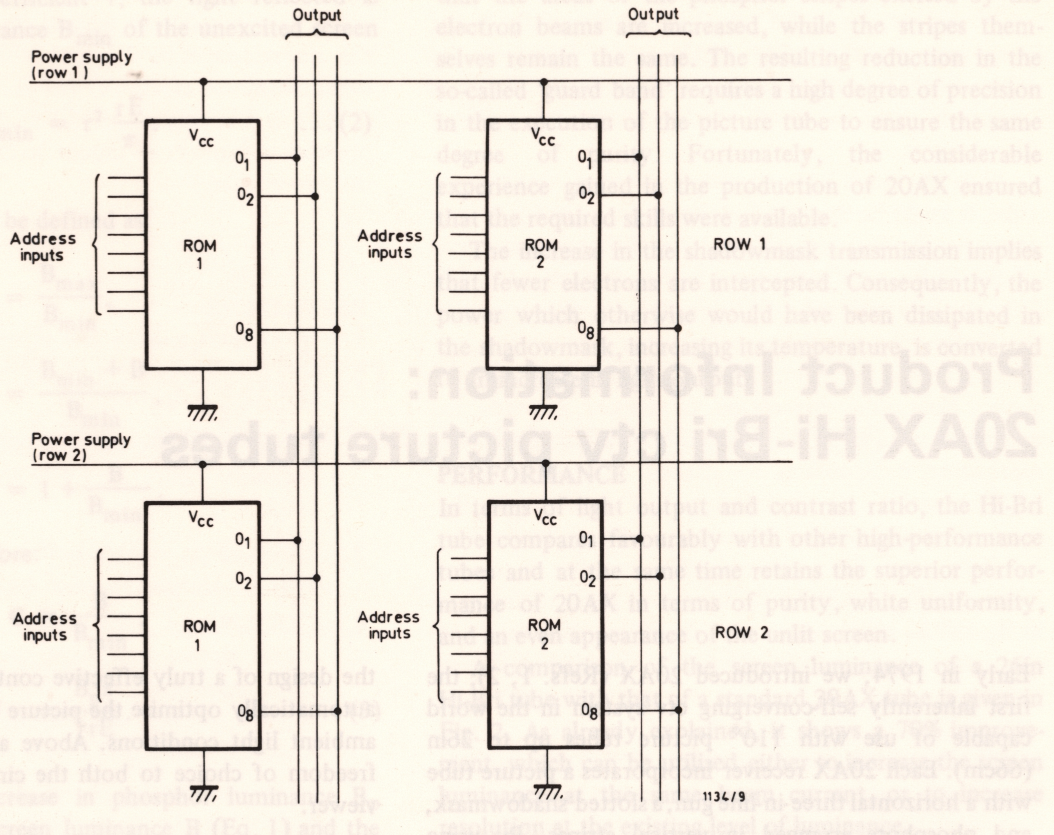

Output
Power supply (row 1)
Vcc
O1
O2
Address inputs
ROM 1
O8
Output
Vcc
O1
O2
Address inputs
ROM 2
O8
ROW 1
Power supply (row 2)
Vcc
O1
O2
Address inputs
ROM 1
O8
Vcc
O1
O2
Address inputs
ROM 2
O8
ROW 2
1134/9

Fig.9 – Word-organised memory system

Low-duty-cycle system

In many applications a memory circuit only needs to be turned on for short periods, during which data is taken from the memory to be used or stored elsewhere. Fig.10 shows a generalised timing diagram for a system in which a memory circuit is on for only T_e seconds during a particular system cycle. Suppose this system cycle to be T_a seconds in duration, and that N_a active cycles are repetitively followed by N_d 'dead' cycles when the IC is not used at all. Thus the average power consumption if power strobing is used is given by:

$$\text{Average power consumption} = \frac{P_1\,T_e\,N_a}{T_a\,(N_a + N_d)},$$

where P_1 is the power consumption of the memory IC.

The saving in power compared with the same memory device without power strobing is given by:

$$\text{Power saving} = P_1 \left\{ 1 - \frac{T_e\,N_a}{T_a\,(N_a + N_d)} \right\}.$$

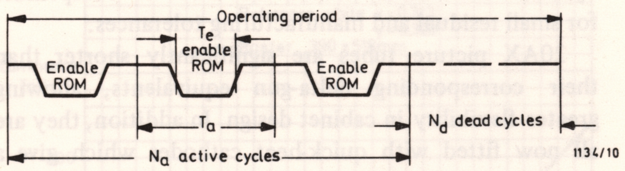

Operating period
Te
enable ROM
Enable ROM
Enable ROM
Ta
Nd dead cycles
Na active cycles
1134/10

Fig.10 – Timing waveforms for a low-duty-cycle memory system

The percentage power saving is given by:

$$\text{Percentage saving} = 100 \left\{ 1 - \frac{T_e\,N_a}{T_a\,(N_a + N_d)} \right\}\%.$$

As an example, consider a system in which $T_e = 200$ns, $T_a = 1\mu$s, and $N_d = 2N_a$. The percentage power saving is then greater than 93%.

Product Information: 20AX Hi-Bri ctv picture tubes

Early in 1974, we introduced 20AX (Refs. 1, 2), the first inherently self-converging ctv system in the world capable of use with 110° picture tubes up to 26in (66cm). Each 20AX receiver incorporates a picture tube with a horizontal three-in-line gun, a slotted shadowmask, and phosphors arranged in vertical stripes. By using specially-designed saddle-wound deflection yokes, the complex dynamic correction circuits required in comparable delta-gun-tube receivers are eliminated; the only dynamic corrections needed are those to compensate for small residual and manufacturing tolerances.

20AX picture tubes are significantly shorter than their corresponding delta-gun equivalents, allowing greater flexibility in cabinet design. In addition, they are all now fitted with quick-heat cathodes which give a picture within 5s of switch-on (Ref. 3), and are optimised for minimum moiré. Soon, all tubes in the range will be available in Soft-Flash technology, an improvement which effectively limits the energy dissipated during a flashover, and hence reduces the possibility of damage to low-voltage receiver circuitry (Ref. 4).

The latest innovation in 20AX is the introduction of Hi-Bri versions (Ref. 5) of the standard tube range; these offer a 70% increase in brightness with no loss in contrast. This increase in light output efficiency can be utilised in a number of ways. An obvious application is in improving the picture brightness in areas of high ambient illumination such as in well-lit rooms or shop windows, or when viewing in daylight. Furthermore, users not requiring an increase in screen luminance benefit from an improvement in resolution and a reduction in power consumption, resulting from operation at lower beam current.

The availability of extra screen luminance also permits the design of a truly effective control circuit which can automatically optimise the picture brightness for varying ambient light conditions. Above all, it provides a wide freedom of choice to both the circuit designer and the viewer.

PRINCIPLES OF HI-BRI

The screen of a picture tube is sketched in section in Fig. 1. If the phosphor layer is producing a luminance B_p, then the luminance B of the screen seen through a faceplate of transmission factor τ is:

$$B = \tau B_p . \quad (\tau < 1) \qquad \ldots(1)$$

If the ambient illumination is E, the light reaching the phosphor layer is τE. Assuming the phosphor layer has a reflection coefficient r, the light reflected is $\tau rE/\pi$, and the luminance B_{min} of the unexcited screen is:

$$B_{min} = \tau^2 \frac{rE}{\pi} . \qquad \ldots(2)$$

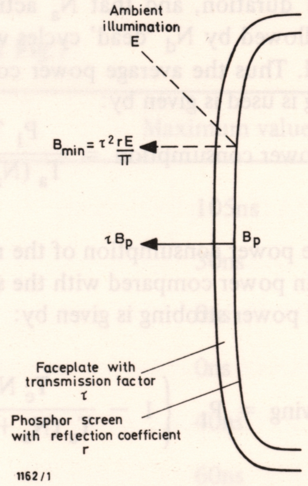

Ambient illumination E
$B_{min} = \tau^2 \frac{rE}{\pi}$
τB_p
B_p
Faceplate with transmission factor τ
Phosphor screen with reflection coefficient r
1162/1

Fig. 1 — Section through screen of picture tube, defining parameters used

The contrast C can be defined as:

$$C = \frac{B_{max}}{B_{min}},$$

$$= \frac{B_{min} + B}{B_{min}},$$

$$= 1 + \frac{B}{B_{min}} .$$

Usually $C \gg 1$, therefore:

$$C \simeq \frac{B}{B_{min}},$$

$$= \frac{B_p \pi}{\tau rE} . \qquad \ldots(3)$$

Note that an increase in phosphor luminance B_p increases both the screen luminance B (Eq. 1) and the contrast C (Eq. 3). An increase in the faceplate transmission τ also increases the luminance but results in a loss of contrast (Eq. 3). Furthermore, if the phosphor luminance B_p is increased by a factor k, then, to obtain the same contrast, the faceplate transmission τ needs to be increased by a factor k. Then the new screen luminance B' becomes, from Eq. 1, $(\tau k) \times (kB_p) = k^2 \tau B_p = k^2 B$.

THE HI-BRI TUBE

In the design of the Hi-Bri tube, the aim was to obtain a large increase in the screen luminance and at the same time retain all the attributes of the standard 20AX tube. Of all the possible approaches, an increase in the shadowmask transmission appeared the most advantageous. Accordingly, the Hi-Bri tube is provided with a shadowmask transmission 30% greater than the standard 20AX tube. The contrast is maintained at the same level as for standard 20AX by increasing the glass transmission by the same factor. The resulting luminance is increased by 1.3 x 1.3 = 1.69; that is nearly 70%. Measurements indicate that in fact the contrast is not only maintained, but is increased by 7%.

Achieving the increase in the faceplate transmission is a relatively simple matter. However, the increase in the shadowmask transmission is a much more serious operation. An obvious consequence of such a step is that the areas of the phosphor stripes excited by the electron beams are increased, while the stripes themselves remain the same. The resulting reduction in the so-called 'guard band' requires a high degree of precision in the execution of the picture tube to ensure the same degree of purity. Fortunately, the considerable experience gained in the production of 20AX ensured that the required skills were available.

The increase in the shadowmask transmission implies that fewer electrons are intercepted. Consequently, the power which otherwise would have been dissipated in the shadowmask, increasing its temperature, is converted to an increase in light output.

PERFORMANCE

In terms of light output and contrast ratio, the Hi-Bri tube compares favourably with other high-performance tubes and at the same time retains the superior performance of 20AX in terms of purity, white uniformity, and an even appearance of the unlit screen.

A comparison of the screen luminance of a 26in Hi-Bri tube with that of a standard 20AX tube is given in Fig. 2. As already explained, it shows a 70% improvement, which can be utilised either to increase the screen luminance at the same beam current, or to increase resolution at the existing level of luminance.

The colour purity in the Hi-Bri tube is good. As a result of the higher precision in the tube manufacture,

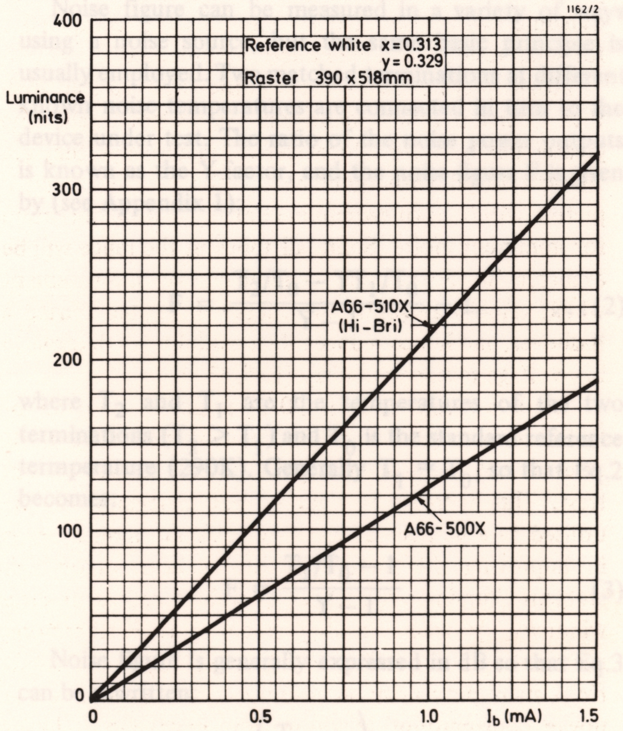


Fig. 2 — Comparison of luminance of standard 20AX tube with that of Hi-Bri tube

no difficulties are encountered in purity adjustment. In every respect, the Hi-Bri tube behaves essentially in the same manner as existing 20AX tubes. However, the substantially-increased luminance offers the possibility of operation over a much wider range of ambient illumination.

With the much higher screen luminance of the Hi-Bri tube, it might be thought that flicker would be a problem. However, for the same contrast, the flicker characteristic of the Hi-Bri tube is the same as that of standard 20AX. This can be explained as follows. The phosphors used in the Hi-Bri tube are the same as those used in standard 20AX, hence the flicker-producing mechanism is the same. Now, the perception of flicker depends on contrast, and to a large extent the accommodation mechanism compensates for changes in absolute levels of illumination. Eq. 3 indicates that to maintain the same contrast C with an increase in ambient illumination E, there must be a corresponding increase in screen luminance B_p. In the Hi-Bri tube, this required increase in B_p can be obtained without degrading the quality of the image because the tube has a greater inherent brightness range.

A SOLUTION WITHOUT COMPROMISE

The Hi-Bri version of 20AX represents a significant step forward in the continuous effort to increase the energy conversion efficiency of colour picture tubes. By improving the precision of the technological processes, it has been possible to increase the light output by 70%, the contrast ratio by 7%, and at the same time retain all other attributes of 20AX. The increased output may be utilised in a variety of ways, but above everything else it provides a freedom of choice to the circuit designer and the viewer alike.

REFERENCES

1. 'The 20AX system and picture tube: deflection in the 20AX system', Technical Note 13, TP1478, Mullard Limited, 1974.
2. '20AX 110° colour television: a brief outline', Technical Note 27, TP1500, Mullard Limited, 1975.
3. 'Quick-vision tv picture tubes', Technical Note 69, TP1637, Mullard Limited, 1977.
4. CIUCIURA, A, 'Soft-Flash: a new development in colour picture tube technology', **Mullard Technical Communications**, Vol. 14, No. 135, July 1977, pp 201 to 208, and Technical Note 59, TP1591, Mullard Limited, 1977.
5. 'Hi-Bri colour tv picture tubes: a further development in 20AX', Technical Note 72, TP1655, Mullard Limited, 1977.

Design and application information for broadband solid-state noise sources

S.R. LONGLEY,
Philips Research Laboratories, Redhill

This article explains why solid-state noise sources are finding an increasing variety of applications and are preferred to other conventional noise sources for many purposes. The BAT31 noise diode is then described; it has a frequency range of 1Hz to 40GHz with a typical excess noise ratio of 34dB. A study of the characteristics of the BAT31 is reported and attention is given to its operation.

INTRODUCTION

One of the most important parameters in microwave communications and radar systems is radio-frequency noise in the receiver. It is often desirable to monitor equipment parameters during use so that changes in system performance can be determined. Noise generators have applications in this field, to indicate system noise figure and gain variations.

The output noise of a system arises from two sources: the input noise amplified by the gain of the system, and the noise generated within the system itself. Therefore, to assess the performance of the system, the input termination must be standardised and a parameter obtained that is independent of the numerical values of gain and bandwidth. Noise figure is such a parameter and it can be conveniently measured using a noise generator.

DEFINITION OF NOISE FIGURE

Noise figure is defined as follows:

noise figure of a two-port transducer =

$$= \frac{\text{signal power input/noise power input}}{\text{signal power output/noise power output}}, \qquad \ldots(1)$$

with the source terminated at 290K (17°C).

Noise figure can be measured in a variety of ways using a noise source, but the same basic principle is usually employed. Two matched terminations at different known noise temperatures are connected in turn to the device under test. The ratio of the noise power outputs is known as the Y-factor, and the noise figure F is given by (see Appendix 1):

$$F = \frac{T_2/T_0 - YT_1/T_0}{Y - 1} + 1, \qquad \ldots(2)$$

where T_2 and T_1 are the temperatures of the two terminations ($T_2 > T_1$) and T_0 is the standard reference termperature (290K). Generally $T_1 \simeq T_0$, so that Eq.2 becomes:

$$F = \frac{T_2/T_0 - 1}{Y - 1} \qquad \ldots(3)$$

Noise figure is generally expressed in dB so that Eq.3 can be rewritten:

$$F(\mathrm{dB}) = 10\log\left(\frac{T_2}{T_0} - 1\right) - 10\log(Y - 1). \qquad \ldots(4)$$

The excess noise ratio (E.N.R.) is the most convenient and commonly used expression to describe the output of noise generators because its value does not depend on the bandwidth. The E.N.R. is the ratio in dB of the excess noise temperature relative to T_0, that is:

$$\text{E.N.R.} = 10 \log \left(\frac{T - T_0}{T_0} \right), \qquad \ldots(5)$$

where T is the noise temperature of the generator.

TYPES OF NOISE SOURCE

There are three types of noise source: gas tubes containing a rare gas at low pressure, solid-state sources based on avalanche diodes, and 'hot and cold' loads.

Hot and cold loads are used mainly where very precise measurements need to be performed; thus, for instance, they are used as measurement standards for the calibration of other types of noise source.

Gas tubes are the traditional type of noise source, but their use is now becoming increasingly limited. Hot and cold loads tend to be preferred for very precise work, and outside the laboratory the durability and versatility of solid-state noise sources means that they are usually preferred to gas tubes.

Solid-state noise sources are used in an increasingly wide range of applications. They are small, rugged, and inexpensive, while producing a high output level for a small power consumption. They have several advantages, including a higher excess noise ratio and a lower operating voltage. Also, they have a wider frequency band since gas tubes are normally waveguide-mounted while solid-state sources are more suitable for incorporation into other microwave transmission media.

Solid-state noise sources are semiconductor pn junction diodes biased into reverse breakdown, and they generate random noise over a wide frequency range. The noise is initiated by thermal, photon, or induced current in the avalanche region liberating an electron (hole) which is accelerated by the electric field. The electron (hole) has sufficient energy to remove an electron from the covalent bond, thus producing an electron-hole pair. Each electron and hole continues under the influence of the electric field and further collisions occur before the electrons and holes reach the zone boundaries. The randomness of this multiplication process produces random fluctuations in the avalanche current.

APPLICATIONS OF SOLID-STATE NOISE SOURCES

Noise figure is generally measured by introducing a known level of noise into the system and comparing it with the internal noise of the system. The noise is gated into the system and the output, which now also contains the system internal noise, is passed to a square-law detector. The detector provides a coherent signal at the gate frequency, which is then filtered to remove it from the remaining noise. A narrowband filter centred on the gate frequency is used, and the narrower the bandwidth of the filter, the lower the level of noise that needs to be introduced into the system.

The noise figure can now be easily determined. The pulsed test noise is switched on and the output from the filter is passed to a voltmeter. The output from the filter with no test noise is then also introduced into the system. The noise figure can be calculated from the two recorded voltmeter readings as follows:

$$\text{noise figure} = C\,\frac{\text{(system noise + test noise) reading}}{\text{system noise reading}}$$

where C is a constant determined by calibrating the equipment. An adaptation of this method, in which an attenuator is used and the noise figure is obtained in dB, is discussed in Appendix 2.

However, alternative methods of inserting test noise can be more appropriate, particularly in radar system applications. For instance, a search or surveillance radar can be tested by introducing a narrow noise pulse, synchronised to the pulse rate of the transmitter, at a time corresponding to the maximum range of the radar. The noise causes a circle to appear at the maximum-range position on the plan position indicator (PPI) of the radar. If the ring is bright and well-defined, the radar is operating correctly and is set up for optimum detection of targets. However, if the noise ring becomes diffuse and ill-defined, then the radar is not operating correctly and appropriate action should be taken. This enables gradual deterioration of the system to be monitored while it is being operated.

Noise sources can also be used to monitor the performance of a tracking radar which has two receivers. The important characteristics of a tracking radar are noise figure, gain-tracking, and phase-tracking. The noise source is connected to the input of each receiver in an identical manner, and the outputs of the receivers are fed to a hybrid junction through lines of equal electrical length, as shown in Fig.1. The output of the junction is fed to a narrowband amplifier tuned to the gate frequency. The noise figure of each channel can then be calculated as outlined previously.

To monitor gain-tracking, the test noise is switched alternately into one receiver and then the other. The output of the amplifier is rectified and then passed through a filter tuned to the switching frequency. Zero output indicates perfect gain-tracking, while the amplitude of the output is proportional to gain-track.

Phase-tracking is monitored by feeding the test noise to both receivers simultaneously. Zero output from the hybrid junction indicates perfect phase-tracking, while any error is proportional to the output signal from the junction.

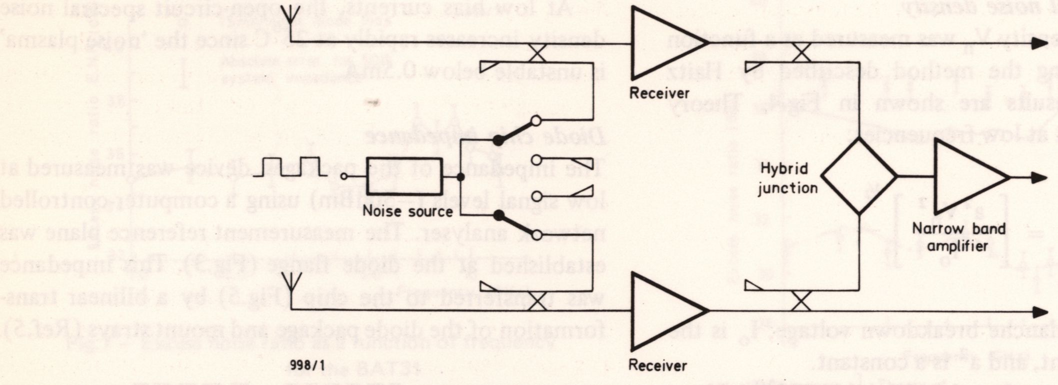


Fig.1 — The use of a noise source to monitor a tracking radar

Solid-state noise sources can be used to check all forms of radar and microwave communications systems. They can be used to determine the noise figure of amplifiers and mixers, and also the gain of a receiver. They are ideally suited to portable fault-finding equipment and their reliable operation under adverse conditions makes them particularly useful for built-in test equipment (BITE). They can also be used for electronic counter-measures such as the jamming of enemy radar by noise modulation of microwave amplifiers. A comprehensive survey of the applications of solid-state noise sources has been made in Ref.1.

DESIGN INFORMATION ON BAT31

The BAT31 is an epitaxial planar passivated reach-through silicon pn diode with a slightly graded junction (Fig.2). It is current-controlled and operated at avalanche breakdown. The BAT31 is an effective noise generator from 1Hz to 40GHz. It is normally operated at an avalanche d.c. current of between 15 and 25mA, where it has a broadband flat noise characteristic with excess noise ratios of greater than 34dB over a frequency range of 10MHz to 12GHz.

The BAT31 is mounted in a small ceramic 'pill'-type package, shown in Fig.3, which is compatible with conventional microwave and radio-frequency circuits excepting stripline. In the examples of the operation of the BAT31 discussed here, the load impedance is 50Ω and any necessary matching circuits are included at the interface with the 50Ω transmission line.

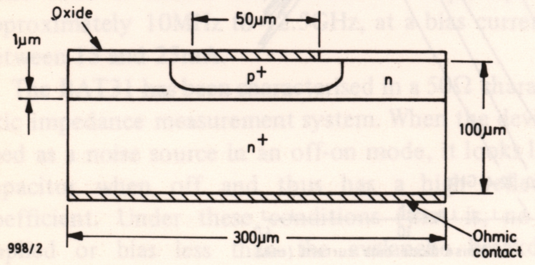


Fig.2 — The noise diode chip

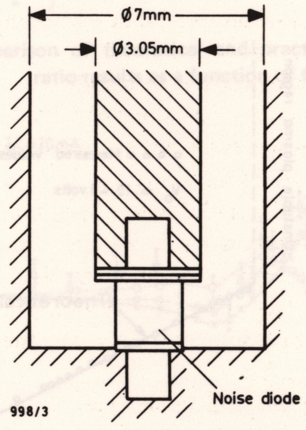


Fig.3 — The noise diode package

Characteristics of BAT31

Table 1 gives brief data on the BAT31; for fuller details refer to the published data.

An investigation of the characteristics of the BAT31 has been reported in Ref.2, part of which is outlined here.

TABLE 1

Quick Reference Data for BAT31

Frequency range		<10Hz to >18GHz
Avalanche voltage	min	17V
	max	22V
Recommended operating current range		0.5 to 40mA
Broadband excess noise ratio typ		34dB

Open-circuit spectral noise density

The spectral noise density V_n was measured as a function of bias current using the method described by Haitz (Ref.3) and the results are shown in Fig.4. Theory (Ref.4) predicts that at low frequencies:

$$V_n = \left[\frac{a^2 V_b{}^2}{I_o}\right]^{\frac{1}{2}},$$

where V_b is the avalanche breakdown voltage, I_o is the avalanche bias current, and a^2 is a constant.

The value of a^2 was found to be 4.4×10^{-20} A/Hz as the best fit with an $I_o{}^{-\frac{1}{2}}$ dependence (Fig.4) for the particular diode studied.

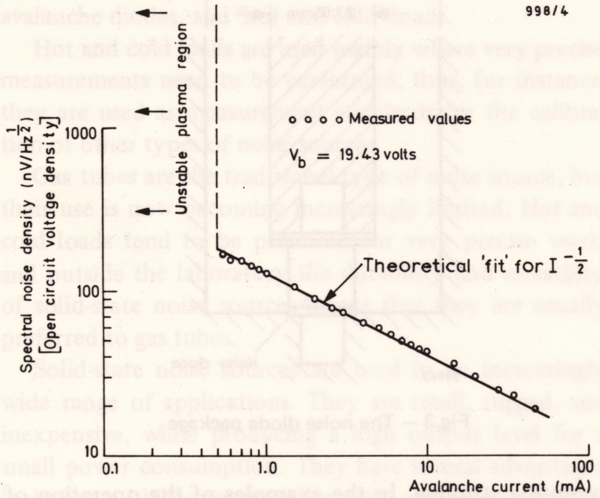


Fig.4 – Open-circuit noise voltage density

At low bias currents, the open-circuit spectral noise density increases rapidly at 25°C since the 'noise plasma' is unstable below 0.5mA.

Diode chip impedance

The impedance of the packaged device was measured at low signal levels (–50dBm) using a computer-controlled network analyser. The measurement reference plane was established at the diode flange (Fig.3). This impedance was transferred to the chip (Fig.5) by a bilinear transformation of the diode package and mount strays (Ref.5).

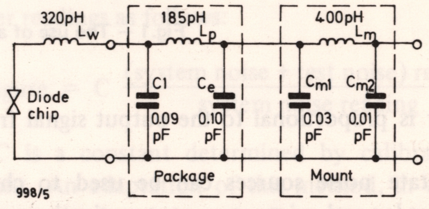


Fig.5 – Lumped equivalent circuit of package and mounted diode

Excess noise ratio

The excess noise ratio at microwave frequencies was measured by reference to a standard noise diode. The packaged device terminated a 50Ω (7mm) transmission line (Fig.3), and the excess noise ratio was measured as a function of bias current with frequency as a parameter; the results are summarised in Fig.6. The results indicate that at bias currents between 15 and 20mA the excess noise ratio is almost independent of frequency between 1 and 12.5GHz. This fact is more clearly indicated in Fig.7 where the excess noise ratio is replotted in the frequency domain with bias current as a parameter.

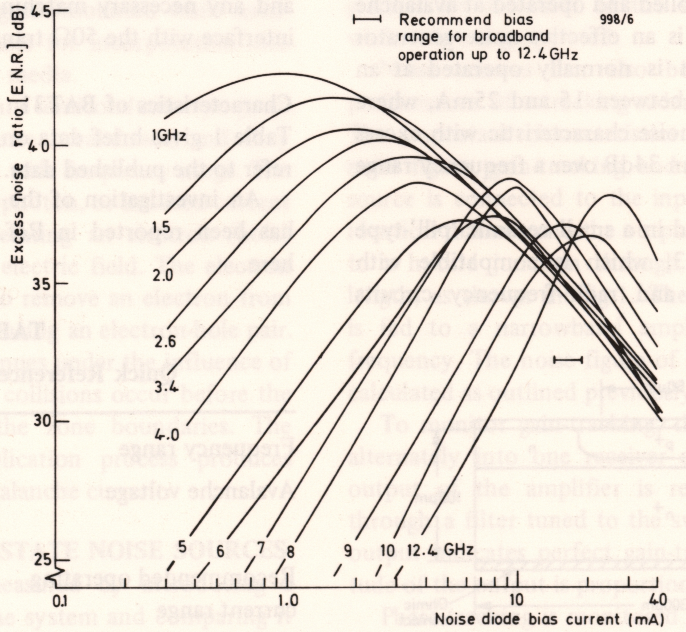


Fig.6 – Variation of excess noise ratio against noise diode bias current for the BAT31

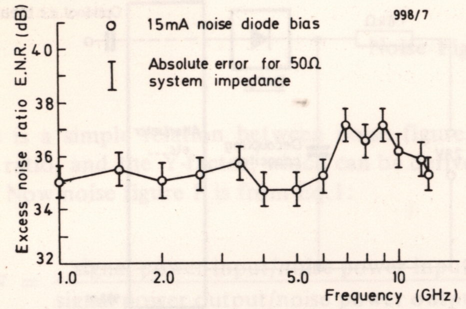


Fig.7 – Excess noise ratio as a function of frequency for the BAT31

Extending the range of frequency independence

Fig.8 shows the experimental results plotted against frequency for two different values of bias current. Also shown for each current value are the theoretical curves derived for pn diodes by an extension of the analysis by Pal *et al* (Ref.6); it can be seen that they are in close agreement with the measured results. An ideal noise source would have an excess noise ratio totally independent of frequency. The close agreement of the theoretical and measured results indicates that this theory can be used to design a diode mount arrangement with a flatter frequency response. The impedance seen by the diode can be altered by using the technique of device embedding. Fig.9 shows that the theoretical curve for the device half-embedded is flatter than that for the device unembedded; however, the full-embedded curve indicates over-compensation. Therefore, the optimum frequency response will be obtained with the diode embedded between these two levels.

OPERATION OF BAT31

The BAT31 noise diode produces white noise over a frequency range of 1Hz to 40GHz and thus has a large variety of applications. For example, low frequency noise can be used for the noise modulation of travelling-wave tubes for jamming applications and also in television applications. High frequency noise (20 to 40GHz), in contrast, has applications for noise generation in radiometer systems for radio astronomy (Ref.7). The BAT31 is particularly useful as a noise source since the excess noise ratio is almost independent of frequency from approximately 10MHz to 12.5GHz, at a bias current of between 15 and 25mA.

The BAT31 has been characterised in a 50Ω characteristic impedance measurement system. When the device is used as a noise source in an off-on mode, it looks like a capacitor when off and thus has a high reflection coefficient. Under these conditions (that is, no bias applied or bias less than the avalanche breakdown voltage), the noise source should look like a matched load at temperature T_0. Therefore, sufficient attenuation is required to provide the desired match to 50Ω and thus an additional microwave component is required such as an attenuator, isolator, or directional coupler.

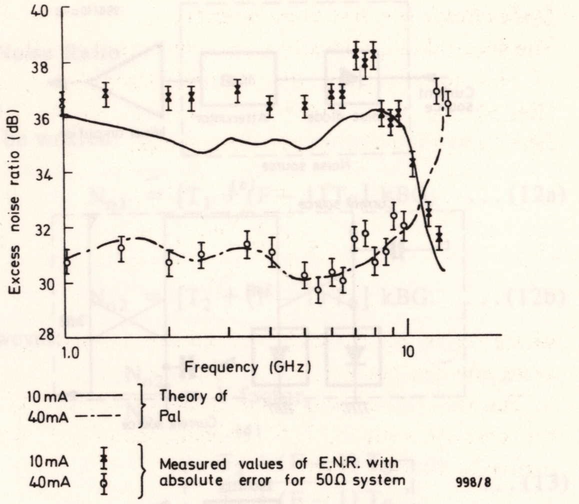


Fig.8 – Comparison of theoretical and practical excess noise ratio results as a function of frequency

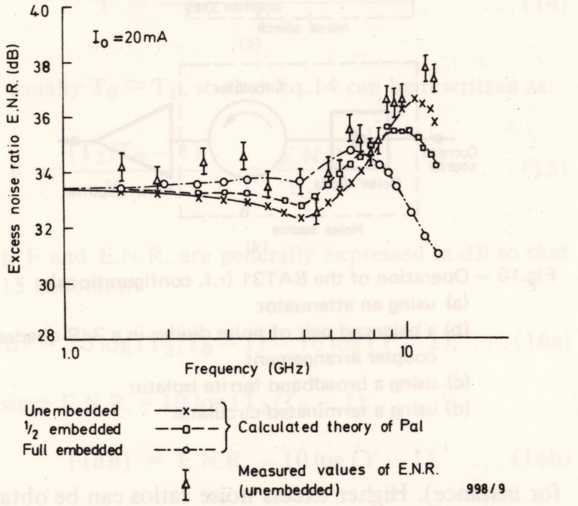


Fig.9 – Comparison of practical excess noise ratio results and theoretical predictions (for the device embedded and unembedded) as a function of frequency

For the broadest operating frequency range, an attenuator of at least 14dB and with a v.s.w.r. of less than 1.2:1 is recommended, see Fig.10a. This reduces the available excess noise, when the device is switched on, by 14dB but provides a good approximation to a perfect matched load when the device is switched off. The use of a directional coupler with 14 to 20dB of decoupling will give a similar result, but the operating range is reduced to approximately one decade. Higher excess noise ratios can be achieved using a balanced pair of noise diodes in a 3dB quadrature coupler arrangement (Ref.8), as shown in Fig.10b; again, the operating range is reduced to approximately one decade (1 to 10GHz,

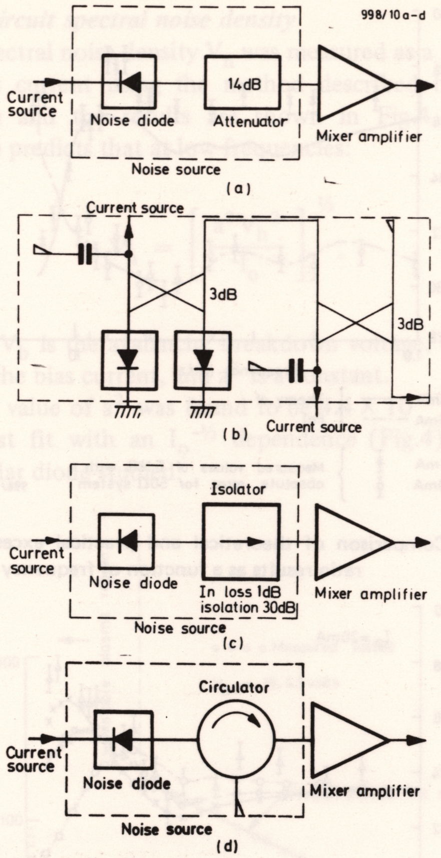


Fig.10 – Operation of the BAT31 (r.f. configurations);
(a) using an attenuator
(b) a balanced pair of noise diodes in a 3dB quadrature coupler arrangement
(c) using a broadband ferrite isolator
(d) using a terminated circulator

for instance). Higher excess noise ratios can be obtained by using a broadband ferrite isolator (peripheral-mode type) or terminated circulator (see Figs.10c and d). Operating bands up to two octaves with a reduction in excess noise ratio of 1dB are possible using this technique. The BAT31 can be pulsed on with a rise time well below 0.5μs, and thus the device can be used when high rates of modulation are required.

The BAT31 should be operated from a constant-current source, but reasonable results can be obtained by using a 28V supply and a metal film resistor in series with the noise diode as in Fig.11. The value of the

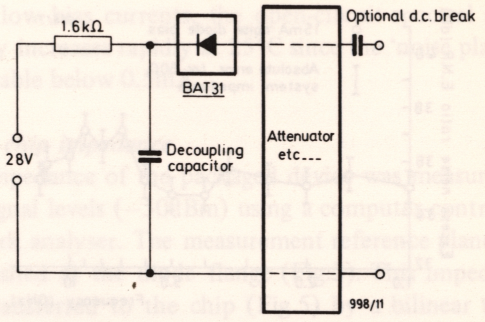


Fig.11 – Operation of the BAT31 from a 28V supply

resistance determines the level of the diode bias current and is typically 1.6kΩ. Power supply decoupling and a d.c. return path should also be incorporated in the design of the mounting.

ACKNOWLEDGEMENTS

The author would like to thank R. Davies of Philips Research Laboratories, Redhill, for technical assistance with this article.

REFERENCES

1. CHASEK, N., 'Avalanche diodes permit in-service measurements of critical parameters in microwave equipment', **Electronics**, January 19, 1970, p.87.
2. LONGLEY, S.R. 'Broadband solid state noise sources', **Mullard Research Laboratories Annual Review**, 1976, p.45.
3. HAITZ, R., 'Noise of a self-sustaining discharge in silicon: low frequency noise studies', **J.A.P.** Vol.18, No.7, June 1976, p.2935.
4. HAITZ, R., VOLTMER, F., 'Noise of a self-sustaining discharge in silicon: studies at microwave frequencies', **J.A.P.**, Vol.39, No.7, June 1968, p.3379.
5. CORBEY, C., GOUGH, R., 'The effects of package and mount parameters on wideband varactor tuned oscillators'. Proc. 4th Biennial Cornell Electrical Engineering Conference, August 14-16, 1973, p.165.
6. PAL, B., SOM, B., ROY, S., 'Effect of finite current multiplication factor in the avalanche zone on the high frequency noise properties of Read diodes', **Proc. IEEE**, August 1976, p.1252.
7. KEEN, N.J., 'Avalanche diode noise sources at short centimeter and millimeter wavelengths', **IEEE Trans.**, March 1976, p.153.
8. KANDA, M., 'An improved solid-state noise source', **IEEE Trans.**, December 1976, p.990.

APPENDIX 1

Noise Figure and Excess Noise Ratio

There is a simple relation between noise figure, excess noise ratio, and the Y-factor, which can be derived from Eq.1. Now noise figure F is from Eq.1:

$$F = \frac{\text{signal power input/noise power input}}{\text{signal power output/noise power output}} \qquad \ldots(6)$$

If S_i is the signal power input, S_o the signal power output, N_i the noise power input, and N_o the noise power output, then Eq.6 can be rewritten:

$$F = \frac{S_i\ N_o}{S_o\ N_i},$$

$$= \frac{1}{G} \cdot \frac{N_o}{N_i}, \qquad \ldots(7)$$

where G is the power gain of the transducer, and thus:

$$N_o = N_iFG. \qquad \ldots(8)$$

Now:

$$N_i = kT_0B, \qquad \ldots(9)$$

where B is the bandwidth, T_0 is the noise temperature of the input termination, and k is Boltzmann's constant.

Substituting Eq.9 into Eq.8, gives

$$N_o = kT_0BFG, \qquad \ldots(10)$$

or:

$$N_o = [T_0 + (F-1)T_0]\ kBG. \qquad \ldots(11)$$

Now, consider two inputs with terminations at different temperature T_1 and T_2 ($T_2 > T_1$), then Eq.11 can be written:

$$N_{o1} = [T_1 + (F-1)T_0]\ kBG, \qquad \ldots(12a)$$

and:

$$N_{o2} = [T_2 + (F-1)T_0]\ kBG. \qquad \ldots(12b)$$

However:

$$\frac{N_{o2}}{N_{o1}} = \text{Y-factor},$$

$$= \frac{T_2 + (F-1)T_0}{T_1 + (F-1)T_0}, \qquad \ldots(13)$$

or:

$$F = \frac{T_2/T_0 - Y(T_1/T_0) - 1}{Y-1}, \qquad \ldots(14)$$

and usually $T_0 \simeq T_1$, so that Eq.14 can be rewritten as:

$$F = \frac{(T_2/T_0 - 1)}{Y-1}, \quad = \frac{\text{E.N.R.}}{Y-1}. \qquad \ldots(15)$$

Both F and E.N.R. are generally expressed in dB so that Eq.15 becomes:

$$F(\text{dB}) = 10\log(T_2/T_0 - 1) - 10\log(Y-1), \qquad \ldots(16a)$$

or, since E.N.R. = 10 log ($T_2/T_0 - 1$):

$$F(\text{dB}) = \text{E.N.R.} - 10\log(Y-1), \qquad \ldots(16b)$$

This expression enables the noise figure of a device to be measured quickly and simply, using a noise generator (see Appendix 2).

APPENDIX 2

Measurement of Noise Figure

Fig.12 shows the arrangement for the measurement of noise figure. The noise diode is turned off so that the device is presented with a matched load at room temperature (assumed to be T_0 = 290K, except in very precise work). The voltmeter is set to a convenient reading and the noise diode is turned on. The reading on the voltmeter is then returned to its previous value by adjusting the r.f. attenuator. The difference between the settings of the attenuator is the Y-factor in dB which is converted into a power ratio and then substituted into Eq.16:

$$F(\mathrm{dB}) = 10 \log (T_2/T_0 - 1) - 10 \log (Y - 1). \quad \ldots (17)$$

This method can be simplified if Y = 2 (or 3dB), when Eq.17 becomes:

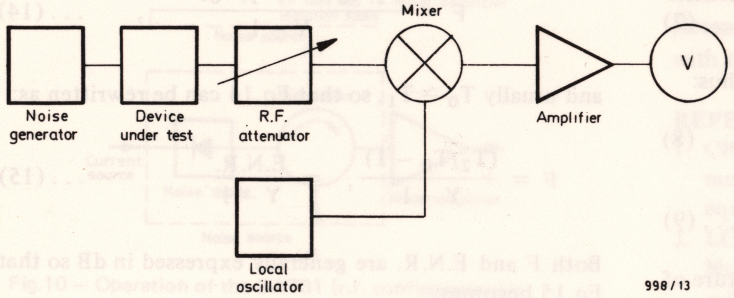
$$F(\mathrm{dB}) = 10 \log (T_2/T_0 - 1), \quad \ldots (18)$$

which is the excess noise ratio of the noise generator. Consequently, if an r.f. attenuator is placed between the noise diode and the device under test and is adjusted so that switching the diode on causes the output at the voltmeter to double, then:

$$F(\mathrm{dB}) = \mathrm{E.N.R.} - x\mathrm{dB}, \quad \ldots (19)$$

where x is the setting on the attenuator.

Measuring noise figure in this manner is extremely convenient but is very dependent on the accuracy of the r.f. attenuator.



998/13 Fig.12 — The measurement of noise figure

TELEVISION SWITCHED-MODE POWER SUPPLY WITH ISOLATION

The fourth article in the current series on television SMPS circuits should have appeared in this issue of Mullard Technical Communications but has been delayed. The article is in preparation for release in the next issue, No.139.